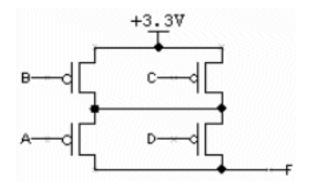6.004 Computation Structures
Spring 2009

CMOS technology

Problem 1. The following diagram shows a schematic for the pulldown circuitry for a particular CMOS gate:

A. ★ What is the correct schematic for the pullup circuitry?

B. ★ Assuming the pullup circuitry is designed correctly, what is the logic function implemented this gate?

C. ★ Assuming the pullup circuitry is designed correctly, when the output of the CMOS gate above is a logic "0", in the steady state what would we expect the voltage of the output terminal to be? What would be the voltage if the output were a logic "1"?
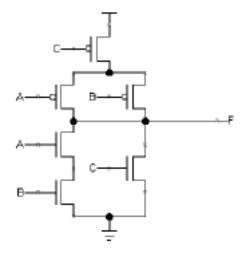

Problem 2. The following diagram shows a schematic for the pullup circuitry for a particular CMOS gate:

A. ★ Draw a schematic for the pulldown circuitry for this CMOS gate.

B. ⭐ Assuming the pulldown circuitry is designed correctly, give an expression for the logic function implemented by this gate.

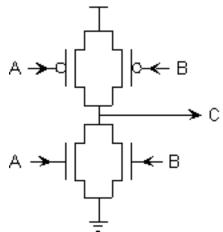Problem 3. Consider the following circuit built from nfets and pfets:

A. ⭐ Can this circuit be used as a CMOS gate? If not, explain why. If so, what function does it compute?

B. ⭐ If we wanted the output voltage to change more quickly when going from a logic "0" to a logic "1", what changes would we make to the fets?

Problem 4. Consider the 4-input Boolean function Y = (A*B) + (C*D) where "*" is AND and "+" is OR.

A. ⭐ Implement the function with a single 4-input CMOS gate and an inverter.
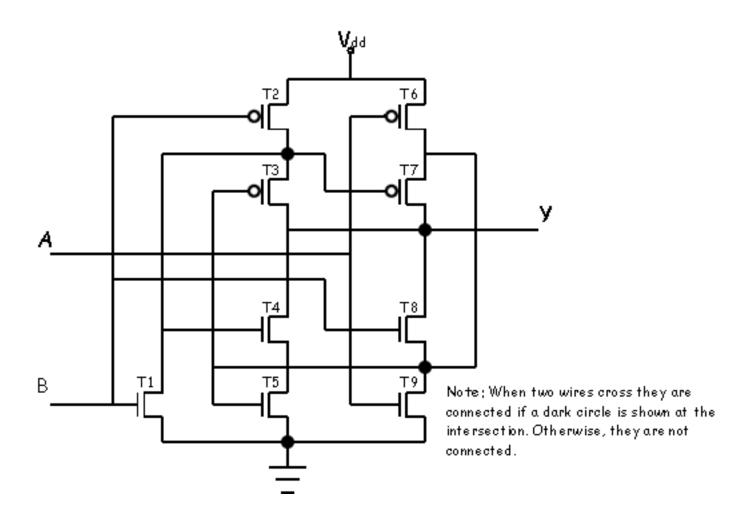

Problem 5. Anna Logue, a circuit designer who missed several early 6.004 lectures, is struggling to design her first CMOS logic gate. She has implemented the following circuit:

Anna has fabricated 100 test chips containing this circuit, and has a simple testing circuit which allows her to try out her proposed gate statically for various combinations of the A and B inputs. She has burned out 97 of her chips, and needs your help before destroying the remaining three. She is certain she is applying only valid input voltages, and expects to find a valid output at terminal C. Anna also keeps noticing a very faint smell of smoke.

A. What is burning out Anna's test chips? Give a specific scenario, including input values together with a description of the failure scenario. For what input combinations will this failure occur?

B. Are there input combinations for which Anna can expect a valid output at C? Explain.

C. One of Anna's test chips has failed by burning out the pullup connected to A as well as the pulldown connected to B. Each of the burned out FETs appears as an open circuit, but the rest of the circuit remains functional. Can the resulting circuit be used as a combinational device whose two inputs are A and B? Explain its behavior for each combination of valid inputs.

D. In order to salvage her remaining three chips, Anna connects the A and B inputs of each and tries to use it as a single-input gate. Can the result be used as a single-input combinational device? Explain.

Problem 6. Occasionally you will come across a CMOS circuit where the complementary nature of the n-channel pull-downs and p-channel pull-ups are not obvious, as in the circuit shown below:

Note: When two wires cross they are connected if a dark circle is shown at the intersection. Otherwise, they are not connected.

A. Construct a table that gives the on-off status of each transistor in the circuit above for all combinations of inputs A and B.

B. Compute the output, Y, for each input combination and describe the function of the above circuit.

Problem 7. In lecture there was a brief overview of the CMOS fabrication process.

A. What keeps the source/drain diffusions of a MOSFET from shorting out to the substrate or to each other?

B. Why does reducing the thickness of the thin oxide layer improve the performance of the mosfets?

C. Why is silicon dioxide (SiO_2) deposited right before a new wiring layer is added to the surface of the wafer?

D. How are connections between the wiring layers made?

E. If one wanted to *increase* I_{DS} for a NFET, how should it's dimensions be changed?

F. Suppose there are two mosfets of width W and length L connected in parallel, i.e., all their terminal connections are identical. Given that I_{DS} of a mosfet is proportional to W/L, what would be the appropriate dimensions for a *single* mosfet that would have the same I_{DS} as the pair connected in parallel?