November 16, 2005 - Quiz #2

Name: _____

Recitation: _____

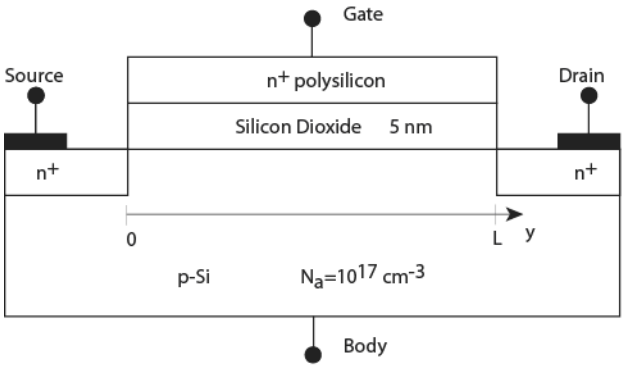
problem	grade
1	
2	
3	
4	
total	

General guidelines (please read carefully before starting):

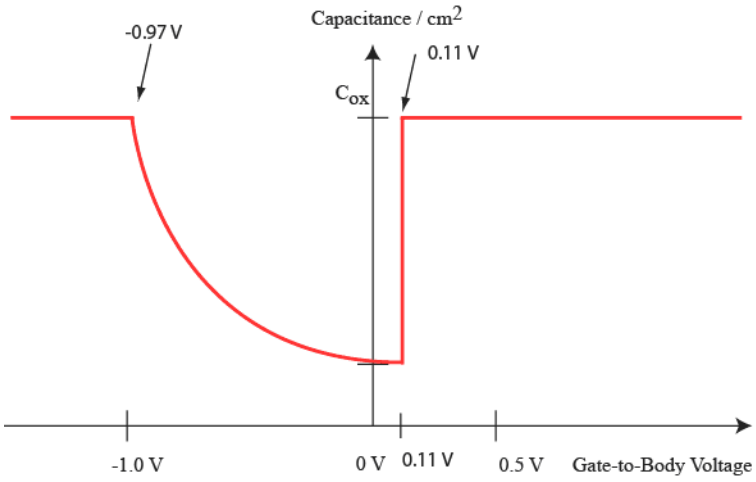
- Make sure to write your name on the space designated above.
- **Open book**: you can use any material you wish.
- All answers should be given in the space provided. Please do not turn in any extra material. If you need more space, use the back of the page.
- You have **120 minutes** to complete your quiz.
- Make reasonable approximations and *state them*, i.e. quasi-neutrality, depletion approximation, etc.
- Partial credit will be given for setting up problems without calculations. **NO** credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. μ_n, I_D, E, etc.
- Every numerical answer must have the proper units next to it. Points will be subtracted for answers without units or with wrong units.
- Use $\phi = 0$ at $n_o = p_o = n_i$ as potential reference.
- Use the following fundamental constants and physical parameters for silicon and silicon dioxide at room temperature:

$n_i = 1 \times 10^{10}\ cm^{-3}$
$kT/q = 0.025\ V$
$q = 1.60 \times 10^{-19}\ C$
$\epsilon_s = 1.05 \times 10^{-12}\ F/cm$
$\epsilon_{ox} = 3.45 \times 10^{-13}\ F/cm$

1. *(30 points)* Below is an n^+ - polysilicon-gate MOSFET. The substrate doping is $N_a = 10^{17}\ cm^{-3}$ and the insulator thickness is 5 nm. The gate length $L = 0.25\ \mu m$ while the gate width is $W = 2.5\ \mu m$. The inversion layer mobility for the MOSFET is $\mu_N = 250\ cm^2/V \cdot s$.



A capacitance voltage curve of the n^+ poly-silicon gate MOSFET was taken by connecting the source, drain and body terminals together. A voltage was applied between the gate and the body.



With the device biased as follows: $V_{BS} = 0\ V$, $V_{DS} = 0.1\ V$, $V_{GS} = \ 1.11\ V$, answer the following questions:

(1a) *(5 points)* Calculate the sheet charge density at the drain end of the device, $Q_n(y = L)$ *(numerical answer expected).*

(1b) *(5 points)* Calculate the electron drift velocity at the drain end of the device, $v_n(y = L)$ *(numerical answer expected).*

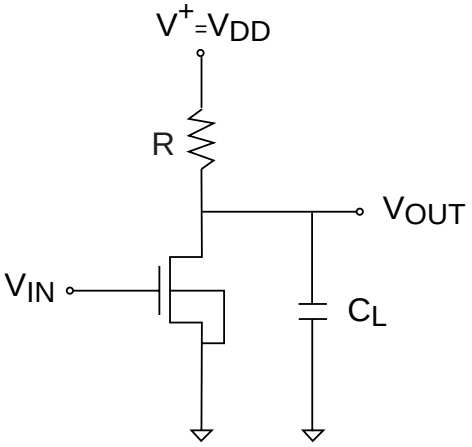
(1c) *(5 points)* Calculate the electron drift velocity in the middle of the channel $v_n(y = L/2)$ *(numerical answer expected).*

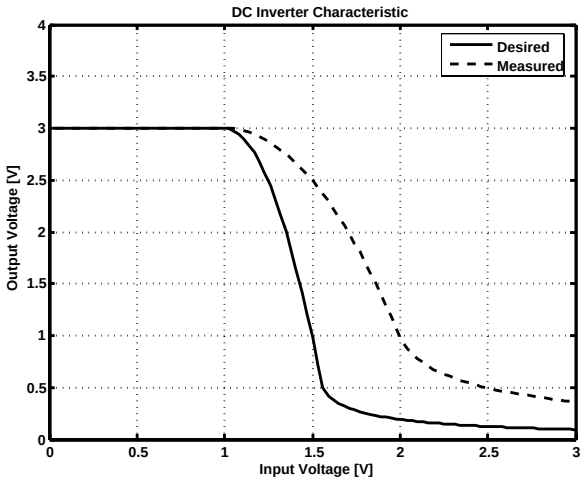
(1d) *(5 points)* This device is now desired to operate at $V_{DS} = 1.8\ V$ and $V_{GS} = 1.35\ V$ with a current $I_D = 1\ mA$. This requires shifting the threshold voltage V_T by means of an applied body voltage, V_{BS}. What is V_T in this situation? *(Numerical answer expected).*

(1e) *(5 points)* For the bias conditions of (1d), compute the sheet charge density at the source end of the channel $Q_n(y = 0)$ *(numerical answer expected).*

(1f) *(5 points)* For the bias conditions of (1d), calculate the electron drift velocity at the source end of the channel, $v_n(y = 0)$ *(numerical answer expected).*

2. *(30 points)* The circuit diagram for an NMOS inverter driving a load capacitance C_L, and a graph of its static input-output characteristics, are shown below. The graph actually shows two sets of characteristics, the desired characteristics and the measured characteristics. The two are different because the actual inverter was not fabricated exactly as it was designed. The point of this problem is to determine what went wrong during fabrication.





The circuit parameters under suspicion are the MOSFET gate width to length ratio, W/L, the MOSFET gate oxide thickness, t_{ox}, the MOSFET body doping level, N_a, and the pull-up resistance, R. Further, assume that one and only one of these four parameters was incorrectly fabricated.

(2a) *(3 points)* From the graph of the desired characteristics, estimate the *desired* threshold voltage V_T of the MOSFET *(numerical answer expected).*

(2b) *(3 points)* From the graph of the measured characteristics, estimate the *actual* threshold voltage V_T of the MOSFET *(numerical answer expected).*

(2c) *(3 points)* From the graph of the desired characteristics, estimate the product of the desired pull-up resistance R and the desired K parameter of the MOSFET (where $K = \frac{W}{L}\mu_n C_{ox}$). That is, estimate the *desired* product RK *(numerical answer expected).*

(2d) *(3 points)* From the graph of the measured characteristics, estimate the product of the actual pull-up resistance R and the actual K parameter of the MOSFET (where $K = \frac{W}{L}\mu_n C_{ox}$). That is, estimate the *actual* product RK *(numerical answer expected).*

In answering the following questions, remember to assume that one and only one of the four parameters was incorrectly fabricated.

(2e) *(3 points)* Could the gate width to length ratio, W/L, have been incorrectly fabricated? Why or why not? If "Yes", is it too big or too small? *(Appropriate explanation expected).*

Circle One: Yes No

(2f) *(3 points)* Could the gate oxide thickness, t_{ox}, have been incorrectly fabricated? Why or why not? If "Yes", is it too big or too small? *(Appropriate explanation expected).*

Circle One: Yes No

(2g) *(3 points)* Could the body doping density, N_a, have been incorrectly fabricated? Why or why not? If "Yes" is it too big or too small? *(Appropriate explanation expected).*

Circle One: Yes No

(2h) *(3 points)* Could the pull-up resistance, R, have been incorrectly fabricated? Why or why not? If "Yes" is it too big or too small? *(Appropriate explanation expected).*

Circle One: Yes No

You observe that when the inverter is driving a known load capacitance C_L, one of the propagation delays (t_{PLH} and t_{PHL}) is not as desired. In particular, the propagation delay from a rising input to a falling output is longer than expected, while the propagation delay from a falling input to a rising output is exactly what was expected.

(2i) *(6 points)* Based on all available evidence, which circuit parameter was incorrectly fabricated? What is the ratio of the actual parameter divided by the desired parameter? *(Appropriate explanation expected).*

3. *(24 points)* An pn diode at a certain forward bias point is characterized by the following values of small-signal equivalent circuit elements:

$$r_d = 25\ \Omega \qquad C_d = 40\ pF$$

At this bias point, the depletion capacitance is negligible with respect to the diffusion capacitance.

In the following questions, you are asked to estimate how the values of these two elements change if the diode is modified in several ways. Assume that in all cases, the diode is ideal, very asymmetric, and that all its behavior is dominated by its lowly doped side. State any other assumptions you need to make.

(3a) *(4 points)* The diode area is doubled. Nothing else is changed. The diode is biased at the *same current* as in the problem statement *(numerical answers expected).*

(3b) *(4 points)* The diode area is doubled. Nothing else is changed. The diode is biased at the *same voltage* as in the problem statement *(numerical answers expected).*

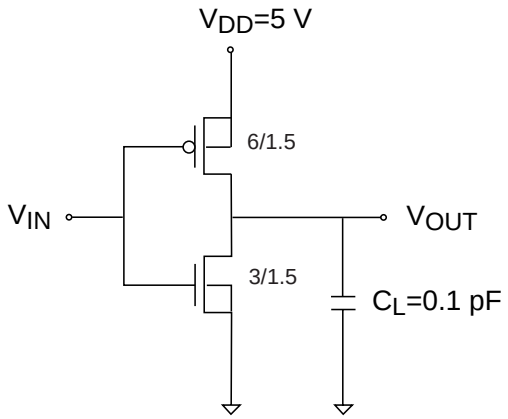
(3c) *(4 points)* The doping level of the lowly doped side is doubled. Nothing else is changed. The diode is biased at the *same current* as in the problem statement *(numerical answers expected).*

(3d) *(4 points)* The doping level of the lowly doped side is doubled. Nothing else is changed. The diode is biased at the *same voltage* as in the problem statement *(numerical answers expected).*

(3e) *(4 points)* The thickness of the lowly doped side is doubled. Nothing else is changed. The diode is biased at the *same current* as in the problem statement *(numerical answers expected).*

(3f) *(4 points)* The thickness of the lowly doped side is doubled. Nothing else is changed. The diode is biased at the *same voltage* as in the problem statement *(numerical answers expected).*

4. *(16 points)* Consider a CMOS logic gate driving a capacitive load C_L. The inverter is made with minimum size transistors, as sketched below:



In the above diagram, the two numbers next to each transistor give its gate dimensions (width/length) in microns. In solving this problem, assume that C_L is the dominant capacitance in this circuit. All other capacitances can be neglected next to C_L.

The technology is defined by the following circuit parameters plus other geometrical parameters:

Parameter Name	HSPICE Symbol	NMOS	PMOS	units
Zero bias threshold voltage	VTO	0.75	-0.75	V
Oxide thickness	TOX	1.5E-08	1.5E-08	m
Transconductance parameter μC_{ox}	KP	100E-06	50E-06	A/V^2
Channel-length modulation parameter	LAMBDA	7E-02$\frac{1.5}{L(\mu m)}$	7E-02$\frac{1.5}{L(\mu m)}$	V^{-1}
Zero bias planar bulk depletion capacitance	CJ	1E-04	3E-04	F/m^2
Zero bias sidewall bulk depletion capacitance	CJSW	5E-10	3.5E-10	F/m
Bulk junction potential	PB	0.9	0.9	V
Planar bulk junction grading coefficient	MJ	0.5	0.5	dimensionless
Sidewall bulk junction grading coefficient	MJSW	0.33	0.33	dimensionless
Diffusion length	L_{diff}	4.5	4.5	μm
Minimum transistor length	L_{min}	1.5	1.5	μm
Minimum transistor width	W_{min}	3	6	μm

(4a) *(8 points)* Estimate the energy stored in the load capacitor when the output is HI *(numerical answer expected)*.

(4b) *(8 points)* Estimate the power dissipated by this inverter when it is run at 100 MHz *(numerical answer expected)*.