# 6.012 Microelectronic Devices and Circuits

Formula Sheet for the Final Exam, Fall 2009

## Parameter Values:

$q = 1.6x10^{-19}\ Coul$
$\varepsilon_o = 8.854x10^{-14}\ F/cm$
$\varepsilon_{r,Si} = 11.7, \quad \varepsilon_{Si} \approx 10^{-12}\ F/cm$
$n_i[Si@R.T] \approx 10^{10}\ cm^{-3}$
$kT/q \approx 0.025\ V; \quad (kT/q)\ln 10 \approx 0.06\ V$
$1\ \mu m = 1x10^{-4}\ cm$

## Periodic Table:

| III | IV | V |
|---|---|---|
| B | C | N |
| Al | Si | P |
| Ga | Ge | As |
| In | Sn | Sb |

## Drift/Diffusion:

Drift velocity: $\bar{s}_x = \pm\mu_m E_x$

Conductivity: $\sigma = q(\mu_e n + \mu_h p)$

Diffusion flux: $F_m = -D_m \dfrac{\partial C_m}{\partial x}$

Einstein relation: $\dfrac{D_m}{\mu_m} = \dfrac{kT}{q}$

## Electrostatics:

$$\varepsilon\frac{dE(x)}{dx} = \rho(x) \qquad E(x) = \frac{1}{\varepsilon}\int \rho(x)dx$$

$$-\frac{d\phi(x)}{dx} = E(x) \qquad \phi(x) = -\int E(x)dx$$

$$-\varepsilon\frac{d^2\phi(x)}{dx^2} = \rho(x) \qquad \phi(x) = -\frac{1}{\varepsilon}\iint \rho(x)dxdx$$

## The Five Basic Equations:

Electron continuity: $$\frac{\partial n(x,t)}{\partial t} - \frac{1}{q}\frac{\partial J_e(x,t)}{\partial x} = g_L(x,t) - \left[n(x,t)\cdot p(x,t) - n_i^2\right]r(T)$$

Hole continuity: $$\frac{\partial p(x,t)}{\partial t} + \frac{1}{q}\frac{\partial J_h(x,t)}{\partial x} = g_L(x,t) - \left[n(x,t)\cdot p(x,t) - n_i^2\right]r(T)$$

Electron current density: $$J_e(x,t) = q\mu_e n(x,t)E(x,t) + qD_e\frac{\partial n(x,t)}{\partial x}$$

Hole current density: $$J_h(x,t) = q\mu_h p(x,t)E(x,t) - qD_h\frac{\partial p(x,t)}{\partial x}$$

Poisson's equation: $$\frac{\partial E(x,t)}{\partial x} = \frac{q}{\varepsilon}\left[p(x,t) - n(x,t) + N_d^+(x) - N_a^-(x)\right]$$

## Uniform doping, full ionization, TE

n - type, $N_d >> N_a$

$$n_o \approx N_d - N_a \equiv N_D, \quad p_o = n_i^2/n_o, \quad \phi_n = \frac{kT}{q}\ln\frac{N_D}{n_i}$$

p - type, $N_a >> N_d$

$$p_o \approx N_a - N_d \equiv N_A, \quad n_o = n_i^2/p_o, \quad \phi_p = -\frac{kT}{q}\ln\frac{N_A}{n_i}$$

## Uniform optical excitation, uniform doping

$$n = n_o + n' \qquad p = p_o + p' \qquad n' = p' \qquad \frac{dn'}{dt} = g_l(t) - (p_o + n_o + n')n'r$$

Low level injection, $n',p' << p_o + n_o$: $$\frac{dn'}{dt} + \frac{n'}{\tau_{min}} = g_l(t) \quad \text{with} \quad \tau_{min} \approx (p_o r)^{-1}$$

Flow problems (uniformly doped quasi-neutral regions with quasi-static excitation and low level injection; p-type example):

Minority carrier excess: $$\frac{d^2 n'(x)}{dx^2} - \frac{n'(x)}{L_e^2} = -\frac{1}{D_e} g_L(x) \qquad L_e \equiv \sqrt{D_e \tau_e}$$

Minority carrier current density: $$J_e(x) \approx qD_e \frac{dn'(t)}{dx}$$

Majority carrier current density: $$J_h(x) = J_{Tot} - J_e(x)$$

Electric field: $$E_x(x) \approx \frac{1}{q\mu_h p_o}\left[J_h(x) + \frac{D_h}{D_e} J_e(x)\right]$$

Majority carrier excess: $$p'(x) \approx n'(x) + \frac{\varepsilon}{q}\frac{dE_x(x)}{dx}$$

Short base, infinite lifetime limit:

Minority carrier excess: $$\frac{d^2 n'(x)}{dx^2} \approx -\frac{1}{D_e} g_L(x), \quad n'(x) \approx -\frac{1}{D_e}\iint g_L(x)dxdx$$

Non-uniformly doped semiconductor sample in thermal equilibrium

$$\frac{d^2\phi(x)}{dx^2} = \frac{q}{\varepsilon}\left\{n_i\left[e^{q\phi(x)/kT} - e^{-q\phi(x)/kT}\right] - \left[N_d(x) - N_a(x)\right]\right\}$$

$$n_o(x) = n_i e^{q\phi(x)/kT}, \quad p_o(x) = n_i e^{-q\phi(x)/kT}, \quad p_o(x)n_o(x) = n_i^2$$

Depletion approximation for abrupt p-n junction:

$$\rho(x) = \begin{cases} 0 & \text{for} \quad x < -x_p \\ -qN_{Ap} & \text{for} \quad -x_p < x < 0 \\ qN_{Dn} & \text{for} \quad 0 < x < x_n \\ 0 & \text{for} \quad x_n < x \end{cases}$$

$$N_{Ap}x_p = N_{Dn}x_n$$

$$\phi_b \equiv \phi_n - \phi_p = \frac{kT}{q}\ln\frac{N_{Dn}N_{Ap}}{n_i^2}$$

$$w(v_{AB}) = \sqrt{\frac{2\varepsilon_{Si}\,(\phi_b - v_{AB})}{q}\frac{(N_{Ap}+N_{Dn})}{N_{Ap}N_{Dn}}} \qquad \left|E_{pk}\right| = \sqrt{\frac{2q\,(\phi_b - v_{AB})}{\varepsilon_{Si}}\frac{N_{Ap}N_{Dn}}{(N_{Ap}+N_{Dn})}}$$

$$q_{DP}(v_{AB}) = -AqN_{Ap}x_p(v_{AB}) = -A\sqrt{2q\varepsilon_{Si}\,(\phi_b - v_{AB})\frac{N_{Ap}N_{Dn}}{(N_{Ap}+N_{Dn})}}$$

Ideal p-n junction diode i-v relation:

$$n(\text{-}x_p) = \frac{n_i^2}{N_{Ap}}e^{qv_{AB}/kT}, \quad n'(\text{-}x_p) = \frac{n_i^2}{N_{Ap}}\left(e^{qv_{AB}/kT} - 1\right); \qquad p(x_n) = \frac{n_i^2}{N_{Dn}}e^{qv_{AB}/kT}, \quad p'(x_n) = \frac{n_i^2}{N_{Dn}}\left(e^{qv_{AB}/kT} - 1\right)$$

$$i_D = Aqn_i^2\left[\frac{D_h}{N_{Dn}w_{n,eff}} + \frac{D_e}{N_{Ap}w_{p,eff}}\right]\left[e^{qv_{AB}/kT} - 1\right] \qquad w_{m,eff} = \begin{cases} w_m - x_m & \text{if } L_m >> w_m \\ L_m \tanh\left[(w_m - x_m)/L_m\right] & \text{if } L_m \sim w_m \\ L_m & \text{if } L_m << w_m \end{cases}$$

$$q_{QNR,p\text{-}side} = Aq\int_{-w_p}^{-x_p} n'(x)dx, \qquad q_{QNR,n\text{-}side} = Aq\int_{x_n}^{w_n} p'(x)dx,$$

Note: $p'(x) \approx n'(x)$ in QNRs

Large signal BJT Model in Forward Active Region (FAR):
(npn with base width modulation)

$$i_B(v_{BE},v_{CE}) = I_{BS}\left(e^{qv_{BE}/kT}-1\right)$$

$$i_C(v_{BE},v_{BC}) = \beta_F\ i_B(v_{BE},v_{CE})\left[1+\lambda v_{CE}\right] = \beta_F I_{BS}\left(e^{qv_{BE}/kT}-1\right)\left[1+\lambda v_{CE}\right]$$

$$\text{with:}\quad I_{BS} \equiv \frac{I_{ES}}{(\beta_F+1)} = \frac{Aqn_i^2}{(\beta_F+1)}\left(\frac{D_h}{N_{DE}w_{E,eff}}+\frac{D_e}{N_{AB}w_{B,eff}}\right),\quad \beta_F \equiv \frac{\alpha_F}{(1-\alpha_F)},\ \text{and}\quad \lambda \equiv \frac{1}{V_A}$$

$$\text{Also,}\quad \alpha_F = \frac{(1-\delta_B)}{(1+\delta_E)}\quad \text{and}\quad \beta_F \approx \frac{(1-\delta_B)}{(\delta_E+\delta_B)}\quad \text{with}\quad \delta_E = \frac{D_h}{D_e}\cdot\frac{N_{AB}}{N_{DE}}\cdot\frac{w_{B,eff}}{w_{E,eff}}\quad \text{and}\quad \delta_B = \frac{w_{B,eff}^2}{2L_{eB}^2}$$

$$\text{When}\quad \delta_B \approx 0\quad \text{then}\quad \alpha_F \approx \frac{1}{(1+\delta_E)}\quad \text{and}\quad \beta_F \approx \frac{1}{\delta_E}$$

MOS Capacitor:

Flat-band voltage: $V_{FB} \equiv v_{GB}$ at which $\phi(0) = \phi_{p-Si}$ $\quad[\Delta\phi = 0 \quad \text{in Si}]$

$$V_{FB} = \phi_{p-Si} - \phi_m$$

Threshold voltage: $V_T \equiv v_{GC}$ at which $\phi(0) = -\phi_{p-Si} - v_{BC}$ $\quad\left[\Delta\phi = \left|2\phi_{p-Si}\right| - v_{BC} \quad \text{in Si}\right]$

$$V_T(v_{BC}) = V_{FB} - 2\phi_{p-Si} + \frac{1}{C_{ox}^*}\left\{2\varepsilon_{Si}qN_A\left[\left|2\phi_{p-Si}\right| - v_{BC}\right]\right\}^{1/2}$$

Depletion region width at threshold: $\quad x_{DT}(v_{BC}) = \sqrt{\dfrac{2\varepsilon_{Si}\left[\left|2\phi_{p-Si}\right| - v_{BC}\right]}{qN_A}}$

Oxide capacitance per unit area: $\quad C_{ox}^* = \dfrac{\varepsilon_{ox}}{t_{ox}}$ $\quad\left[\varepsilon_{r,SiO_2} = 3.9,\quad \varepsilon_{SiO_2} \approx 3.5x10^{-13}\ F/cm\right]$

Inversion layer sheet charge density: $\quad q_N^* = -C_{ox}^*\left[v_{GC} - V_T(v_{BC})\right]$

Accumulation layer sheet charge density: $\quad q_P^* = -C_{ox}^*\left[v_{GB} - V_{FB}\right)]$

Gradual Channel Approximation for MOSFET Characteristics:
(n-channel; strong inversion; with channel length modulation; no velocity saturation)
Only valid for $v_{BS} \le 0$, $v_{DS} \ge 0$.

$$i_G(v_{GS},v_{DS},v_{BS}) = 0,\qquad i_B(v_{GS},v_{DS},v_{BS}) = 0$$

$$i_D(v_{GS},v_{DS},v_{BS}) = \begin{cases} 0 & \text{for}\quad \left[v_{GS}-V_T(v_{BS})\right] < 0 < \alpha v_{DS} \\ \dfrac{K}{2\alpha}\left[v_{GS}-V_T(v_{BS})\right]^2\left[1+\lambda\left(v_{DS}-v_{DS,sat}\right)\right] & \text{for}\quad 0 < \left[v_{GS}-V_T(v_{BS})\right] < \alpha v_{DS} \\ K\left\{v_{GS}-V_T(v_{BS}) - \alpha\dfrac{v_{DS}}{2}\right\}v_{DS} & \text{for}\quad 0 < \alpha v_{DS} < \left[v_{GS}-V_T(v_{BS})\right] \end{cases}$$

$$\text{with}\quad V_T(v_{BS}) \equiv V_{FB} - 2\phi_{p-Si} + \frac{1}{C_{ox}^*}\left\{2\varepsilon_{Si}qN_A\left[\left|2\phi_{p-Si}\right| - v_{BS}\right]\right\}^{1/2},\quad v_{DS,sat} \equiv \frac{1}{\alpha}\left[v_{GS}-V_T(v_{BS})\right]$$

$$K \equiv \frac{W}{L}\mu_e C_{ox}^*,\qquad C_{ox}^* \equiv \frac{\varepsilon_{ox}}{t_{ox}},\qquad \alpha \equiv 1 + \frac{1}{C_{ox}^*}\left\{\frac{\varepsilon_{Si}qN_A}{2\left[\left|2\phi_{p-Si}\right| - v_{BS}\right]}\right\}^{1/2},\qquad \lambda \equiv \frac{1}{V_A}$$

Large Signal Model for MOSFETs Operated below Threshold (weak inversion):
(n-channel) Only valid for for $v_{GS} \le V_T$, $v_{DS} \ge 0$, $v_{BS} \le 0$.

$$i_G(v_{GS}, v_{DS}, v_{BS}) = 0, \qquad i_B(v_{GS}, v_{DS}, v_{BS}) \approx 0$$

$$i_{D,s-t}(v_{GS}, v_{DS}, v_{BS}) \approx I_{S,s-t}\, e^{q\{v_{GS}-V_T(v_{BS})\}/nkT}\left(1-e^{-qv_{DS}/kT}\right) \quad \text{where } I_{S,s-t} \equiv \frac{W}{2L}\mu_e\left(\frac{kT}{q}\right)^2 \sqrt{\frac{2\varepsilon_{Si} q N_A}{|2\phi_p| - v_{BS}}} = \frac{K_o V_t^2 \gamma}{2\sqrt{|2\phi_p| - v_{BS}}}$$

$$\text{with} \quad V_t \equiv \frac{kT}{q}, \quad K_o \equiv \frac{W}{L}\mu_e C_{ox}^*, \quad \gamma \equiv \frac{\sqrt{2\varepsilon_{Si} q N_A}}{C_{ox}^*}, \quad n \approx 1 + \frac{\gamma}{2\sqrt{|2\phi_p| - v_{BS}}}$$

Large Signal Model for MOSFETs Reaching Velocity Saturation at Small $v_{DS}$:
(n-channel) Only valid for $v_{BS} \le 0$, $v_{DS} \ge 0$. Neglects $v_{DS}/2$ relative to $(v_{GS}-V_T)$.

$$\text{Saturation model:} \quad s_y(E_y) = \mu_e E_y \ \text{ if } E_y \le E_{crit}, \quad s_y(E_y) = \mu_e E_{crit} \equiv s_{sat} \ \text{ if } E_y \ge E_{crit}$$

$$i_G(v_{GS}, v_{DS}, v_{BS}) = 0, \qquad i_B(v_{GS}, v_{DS}, v_{BS}) = 0$$

$$i_D(v_{GS}, v_{DS}, v_{BS}) \approx \begin{cases} 0 & \text{for } \quad (v_{GS}-V_T) < 0 < v_{DS} \\ W\ s_{sat} C_{ox}^*[v_{GS}-V_T(v_{BS})][1+\lambda(v_{DS}-\mathrm{E}_{crit}L)] & \text{for } \quad 0 < (v_{GS}-V_T),\ \mathrm{E}_{crit}L < v_{DS} \\ \dfrac{W}{L}\mu_e C_{ox}^*[v_{GS}-V_T(v_{BS})]v_{DS} & \text{for } \quad 0 < (v_{GS}-V_T),\ v_{DS} < \mathrm{E}_{crit}L \end{cases}$$

$$\text{with} \quad \lambda \equiv 1/V_A$$

CMOS Performance

Transfer characteristic:

$$\text{In general:} \quad V_{LO} = 0, \qquad V_{HI} = V_{\mathrm{DD}}, \qquad I_{ON} = 0, \qquad I_{OFF} = 0$$

$$\text{Symmetry:} \quad V_M = \frac{V_{\mathrm{DD}}}{2} \ \text{ and } \ NM_{LO} = NM_{HI} \quad \Rightarrow \quad K_n = K_{\mathrm{p}} \ \text{ and } \ |V_{Tp}| = V_{Tn}$$

$$\text{Minimum size gate:} \quad L_{\mathrm{n}} = L_p = L_{\min}, \quad W_n = W_{\min}, \quad W_p = (\mu_n/\mu_p)W_n \quad \left[\text{or } W_p = (s_{sat,n}/s_{sat,p})W_n\right]$$

Switching times and gate delay (no velocity saturation):

$$\tau_{Charge} = \tau_{Discharge} = \frac{2C_L V_{DD}}{K_n[V_{DD}-V_{Tn}]^2}$$

$$C_L = n(W_n L_n + W_p L_p)C_{ox}^* = 3nW_{\min}L_{\min}C_{ox}^* \qquad \text{assumes } \mu_e = 2\mu_h$$

$$\tau_{Min.Cycle} = \tau_{Charge} + \tau_{Discharge} = \frac{12nL_{\min}^2 V_{DD}}{\mu_e[V_{DD}-V_{Tn}]^2}$$

Dynamic power dissipation (no velocity saturation):

$$P_{dyn@f_{\max}} = C_L V_{DD}^2 f_{\max} \propto \frac{C_L V_{DD}^2}{\tau_{Min.Cycle}} \propto \frac{\mu_e W_{\min}\varepsilon_{ox} V_{DD}[V_{DD}-V_{Tn}]^2}{t_{ox}L_{\min}}$$

$$PD_{dyn@f_{\max}} = \frac{P_{dyn@f_{\max}}}{\text{InverterArea}} \propto \frac{P_{dyn@f_{\max}}}{W_{\min}L_{\min}} \propto \frac{\mu_e \varepsilon_{ox} V_{DD}[V_{DD}-V_{Tn}]^2}{t_{ox}L_{\min}^2}$$

Switching times and gate delay (full velocity saturation):

$$\tau_{Charge} = \tau_{Discharge} = \frac{C_L V_{DD}}{W_{\min} s_{sat} C_{ox}^{*}\left[V_{DD} - V_{Tn}\right]}$$

$$C_L = n\left(W_n L_n + W_p L_p\right)C_{ox}^{*} = 2nW_{\min}L_{\min}C_{ox}^{*} \qquad \text{assumes } s_{sat,e} = s_{sat,h}$$

$$\tau_{Min.Cycle} = \tau_{Charge} + \tau_{Discharge} = \frac{4nL_{\min}V_{DD}}{s_{sat}\left[V_{DD} - V_{Tn}\right]}$$

Dynamic power dissipation per gate (full velocity saturation):

$$P_{dyn@f_{\max}} = C_L V_{DD}^2 f_{\max} \propto \frac{C_L V_{DD}^2}{\tau_{Min.Cycle}} \propto \frac{s_{sat} W_{\min} \varepsilon_{ox} V_{DD}\left[V_{DD} - V_{Tn}\right]}{t_{ox}}$$

$$PD_{dyn@f_{\max}} = \frac{P_{dyn@f_{\max}}}{\text{InverterArea}} \propto \frac{P_{dyn@f_{\max}}}{W_{\min}L_{\min}} \propto \frac{s_{sat}\varepsilon_{ox}V_{DD}\left[V_{DD} - V_{Tn}\right]}{t_{ox}L^2}$$

Static power dissipation per gate

$$P_{static} = V_{DD}\, I_{D,off} \approx V_{DD}\, \frac{W_{\min}}{L_{\min}} \mu_e V_t^2 \sqrt{\frac{\varepsilon_{Si} q N_A}{2\left|V_{BS}\right|}} \quad e^{\{-V_T\}/nV_t}$$

$$PD_{static} = \frac{P_{static}}{\text{Inverter Area}} \propto \frac{V_{DD}}{L_{\min}^2} \mu_e V_t^2 \sqrt{\frac{\varepsilon_{Si} q N_A}{2\left|V_{BS}\right|}} \quad e^{\{-V_T\}/nV_t}$$

<u>CMOS Scaling Rules</u> - Constant electric field scaling

Scaled Dimensions: $L_{\min} \to L_{\min}/s \qquad W \to W/s \qquad t_{ox} \to t_{ox}/s \qquad N_A \to sN_A$

Scaled Voltages: $V_{DD} \to V_{DD}/s \qquad V_{BS} \to V_{BS}/s$

Consequences: $C_{ox}^{*} \to sC_{ox}^{*} \qquad K \to sK \qquad V_T \to V_T/s$

$\tau \to \tau/s \qquad P_{dyn} \to P_{dyn}/s^2 \qquad PD_{dyn@f_{\max}} \to PD_{dyn@f_{\max}}$

$PD_{static} \to s^2\, e^{(s-1)V_T/s\,n\,V_t}\, PD_{static}$

<u>Device transit times</u>

Short Base Diode transit time: $\tau_b = \dfrac{w_B^2}{2D_{\min,B}} = \dfrac{w_B^2}{2\mu_{\min,B}V_{thermal}}$

Channel transit time, MOSFET w.o. velocity saturation: $\tau_{Ch} = \dfrac{2}{3}\dfrac{L^2}{\mu_{Ch}\left|V_{GS} - V_T\right|}$

Channel transit time, MOSFET with velocity saturation: $\tau_{Ch} = \dfrac{L}{s_{sat}}$

Small Signal Linear Equivalent Circuits:

- p-n Diode ($n^+$-p doping assumed for $C_d$)

$$g_d \equiv \left.\frac{\partial i_D}{\partial v_{AB}}\right|_Q = \frac{q}{kT} I_S e^{qV_{AB}/kT} \approx \frac{qI_D}{kT}, \qquad C_d = C_{dp} + C_{df},$$

where $C_{dp}(V_{AB}) = A\sqrt{\dfrac{q\varepsilon_{Si}N_{Ap}}{2(\phi_b - V_{AB})}}$, and $C_{df}(V_{AB}) = \dfrac{qI_D}{kT}\dfrac{\left[w_p - x_p\right]^2}{2D_e} = g_d\tau_d$ with $\tau_d \equiv \dfrac{\left[w_p - x_p\right]^2}{2D_e}$

- BJT (in FAR)

$$g_m = \frac{q}{kT}\beta_o I_{BS} e^{qV_{BE}/kT}\left[1 + \lambda V_{CE}\right] \approx \frac{qI_C}{kT}, \qquad g_\pi = \frac{g_m}{\beta_o} = \frac{qI_C}{\beta_o kT}$$

$$g_o = \beta_o I_{BS}\left[e^{qV_{BE}/kT} + 1\right]\lambda \approx \lambda I_C \qquad \left(\text{or } \approx \frac{I_C}{V_A}\right)$$

$C_\pi = g_m\tau_b +$ B-E depletion cap. with $\tau_b \equiv \dfrac{w_B^2}{2D_e}$, $\quad C_\mu$ : B-C depletion cap.

- MOSFET (strong inversion; in saturation, no velocity saturation)

$$g_m = K\left[V_{GS} - V_T(V_{BS})\right]\left[1 + \lambda V_{DS}\right] \approx \sqrt{2KI_D}$$

$$g_o = \frac{K}{2}\left[V_{GS} - V_T(V_{BS})\right]^2\lambda \approx \lambda I_D \qquad \left(\text{or } \approx \frac{I_D}{V_A}\right)$$

$$g_{mb} = \eta g_m = \eta\sqrt{2KI_D} \qquad \text{with} \quad \eta \equiv -\left.\frac{\partial V_T}{\partial v_{BS}}\right|_Q = \frac{1}{C_{ox}^*}\sqrt{\frac{\varepsilon_{Si}qN_A}{\left|q\phi_p\right| - V_{BS}}}$$

$C_{gs} = \dfrac{2}{3}WLC_{ox}^*$, $\qquad C_{sb}, C_{gb}, C_{db}$ : depletion capacitances

$C_{gd} = WC_{gd}^*$, where $C_{gd}^*$ is the G-D fringing and overlap capacitance per unit gate length (parasitic)

- MOSFET (strong inversion; in saturation with full velocity saturation)

$$g_m = W s_{sat} C_{ox}^*, \qquad g_o = \lambda I_D = \frac{I_D}{V_A}, \qquad g_{mb} = \eta g_m \quad \text{with} \quad \eta \equiv -\left.\frac{\partial V_T}{\partial v_{BS}}\right|_Q = \frac{1}{C_{ox}^*}\sqrt{\frac{\varepsilon_{Si}qN_A}{\left|q\phi_p\right| - V_{BS}}}$$

$C_{gs} = WLC_{ox}^*$, $\qquad C_{sb}, C_{gb}, C_{db}$ : depletion capacitances

$C_{gd} = WC_{gd}^*$, where $C_{gd}^*$ is the G-D fringing and overlap capacitance per unit gate length (parasitic)

- MOSFET (operated sub-threshold; in forward active region; only valid for $v_{bs} = 0$)

$$g_m = \frac{qI_D}{nkT}, \qquad g_o = \lambda I_D = \frac{I_D}{V_A}$$

$C_{gs} = WLC_{ox}^* \Big/ \sqrt{1 + \dfrac{2C_{ox}^{*2}(V_{GS} - V_{FB})}{\varepsilon_{Si}qN_A}}$, $\qquad C_{db}$ : drain region depletion capacitance

$C_{gd} = WC_{gd}^*$, where $C_{gd}^*$ is the G-D fringing and overlap capacitance per unit gate length (parasitic)

Single transistor analog circuit building block stages    Note: $g_l \equiv g_{sl} + g_{el}$; $g_l' \equiv g_o + g_l$

| BIPOLAR | Voltage gain, $A_v$ | Current gain, $A_i$ | Input resistance, $R_i$ | Output resistance, $R_o$ |
|---|---|---|---|---|
| Common emitter | $-\dfrac{g_m}{[g_o + g_l]} \left(\approx -g_m r_l'\right)$ | $-\dfrac{\beta\, g_l}{[g_o + g_l]}$ | $r_\pi$ | $r_o \left(= \dfrac{1}{g_o}\right)$ |
| Common base | $\dfrac{g_m}{[g_o + g_l]} \left(\approx g_m r_l'\right)$ | $\approx 1$ | $\approx \dfrac{r_\pi}{[\beta + 1]}$ | $\approx [\beta + 1] r_o$ |
| Emitter follower | $\dfrac{[g_m + g_\pi]}{[g_m + g_\pi + g_o + g_l]} \approx 1$ | $\dfrac{\beta\, g_l}{[g_o + g_l]} \approx \beta$ | $r_\pi + [\beta + 1] r_l'$ | $\dfrac{r_t + r_\pi}{[\beta + 1]}$ |
| Emitter degeneracy | $\approx -\dfrac{r_l}{R_F}$ | $\approx \beta$ | $\approx r_\pi + [\beta + 1] R_F$ | $\approx r_o$ |
| Shunt feedback | $-\dfrac{[g_m - G_F]}{[g_o + G_F]} \approx -g_m R_F$ | $-\dfrac{g_l}{G_F}$ | $\dfrac{1}{g_\pi + G_F[1 - A_v]}$ | $r_o \parallel R_F \left(= \dfrac{1}{g_o + G_F}\right)$ |

| MOSFET | Voltage gain, $A_v$ | Current gain, $A_i$ | Input resistance, $R_i$ | Output resistance, $R_o$ |
|---|---|---|---|---|
| Common source | $-\dfrac{g_m}{[g_o + g_l]} \left(= -g_m r_l'\right)$ | $\infty$ | $\infty$ | $r_o \left(= \dfrac{1}{g_o}\right)$ |
| Common gate | $\approx [g_m + g_{mb}] r_l'$ | $\approx 1$ | $\approx \dfrac{1}{[g_m + g_{mb}]}$ | $\approx r_o \left\{1 + \dfrac{[g_m + g_{mb} + g_o]}{g_t}\right\}$ |
| Source follower | $\dfrac{[g_m]}{[g_m + g_o + g_l]} \approx 1$ | $\infty$ | $\infty$ | $\dfrac{1}{[g_m + g_o + g_l]} \approx \dfrac{1}{g_m}$ |
| Source degeneracy (series feedback) | $\approx -\dfrac{r_l}{R_F}$ | $\infty$ | $\infty$ | $\approx r_o$ |
| Shunt feedback | $-\dfrac{[g_m - G_F]}{[g_o + G_F]} \approx -g_m R_F$ | $-\dfrac{g_l}{G_F}$ | $\dfrac{1}{G_F[1 - A_v]}$ | $r_o \parallel R_F \left(= \dfrac{1}{[g_o + G_F]}\right)$ |

OCTC/SCTC Methods for Estimating Amplifier Bandwidth

OCTC estimate of $\omega_{HI}$:
$$\omega_{HI} \le \left[\sum_{\mathrm{i}} [\omega_{\mathrm{i}}]^{-1}\right]^{-1} = \left[\sum_{\mathrm{i}} R_i C_i\right]^{-1}$$

with $R_i$ defined as the equivalent resistance in parallel with $C_i$ with all other parasitic device capacitors ($C_\pi$'s, $C_\mu$'s, $C_{gs}$'s, $C_{gd}$'s, etc.) open circuited.

SCTC estimate of $\omega_{LO}$:
$$\omega_{LO} \ge \sum_{\mathrm{j}} \omega_j = \sum_{\mathrm{j}} \left[R_{\mathrm{j}} C_{\mathrm{j}}\right]^{-1}$$

with $R_j$ defined as the equivalent resistance in parallel with $C_j$ with all other baising and coupling capacitors ($C_I$'s, $C_O$'s, $C_E$'s, $C_S$'s, etc.) short circuited.

Difference- and Common-mode signals

Given two signals, $v_1$ and $v_2$, we can decompose them into two new signals, one ($v_C$) that is common to both $v_1$ and $v_2$, and the other ($v_D$) that makes an equal, but opposite polarity contribution to $v_1$ and $v_2$:

$$v_D \equiv v_1 - v_2 \quad \text{and} \quad v_C \equiv \frac{[v_1 + v_2]}{2} \qquad \longrightarrow \qquad v_1 = v_C + \frac{v_D}{2} \quad \text{and} \quad v_1 = v_C - \frac{v_D}{2}$$

Short circuit current gain unity gain frequency, $f_T$

$$\omega_t \approx \left\{ \begin{array}{cc} g_m / C_{gs} = 3\mu_{Ch}(V_{GS} - V_T)/2L^2 = 3s_{Ch}/2L & \text{MOSFET, no vel. sat.} \\ g_m / C_{gs} = W\, s_{sat} C^*_{ox} / W\, L C^*_{ox} = s_{sat}/L & \text{MOSFET, w. vel. sat.} \\ g_m / (C_\pi + C_\mu); \quad \lim_{I_c \to \infty}\left[ g_m / (C_\pi + C_\mu) \right] \approx 2D_{\min,B}/w_B^2 & \text{BJT, large } I_C \end{array} \right\} = \frac{1}{\tau_{tr}}$$

Revised 12/9/09

6.012 Microelectronic Devices and Circuits
Fall 2009