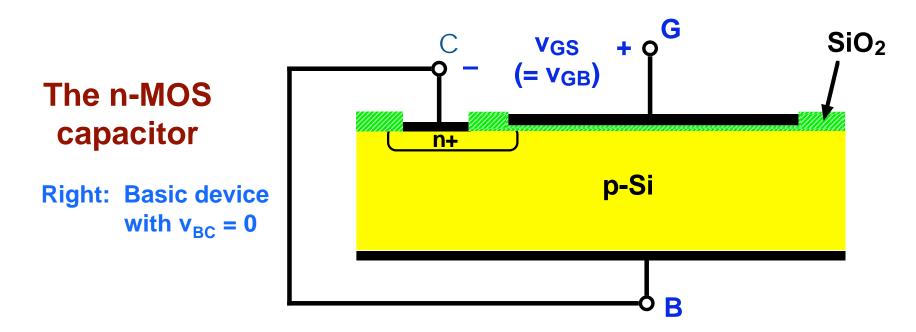
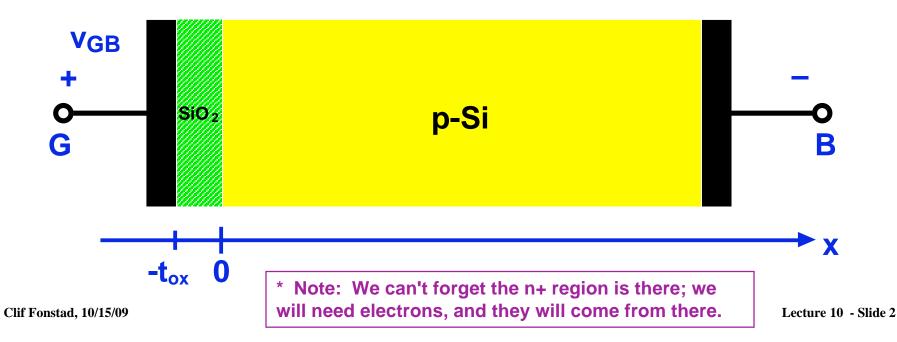


- Charge stores q<sub>G</sub>(v<sub>GB</sub>) from below V<sub>FB</sub> to above V<sub>T</sub> Gate Charge: q<sub>G</sub>(v<sub>GB</sub>) from below V<sub>FB</sub> to above V<sub>T</sub> Gate Capacitance: C<sub>gb</sub>(V<sub>GB</sub>) Sub-threshold charge: q<sub>N</sub>(v<sub>GB</sub>) below V<sub>T</sub>
- 3-Terminal MOS Capacitors Bias between B and C Impact is on V<sub>T</sub>(v<sub>BC</sub>): |2φ<sub>p-Si</sub>| → (|2φ<sub>p-Si</sub>| - v<sub>BC</sub>)
- MOS Field Effect Transistors Basics of model Gradual Channel Model: electrostatics problem normal to channel drift problem in the plane of the channel



**Below: One-dimensional structure for depletion approximation analysis\*** 



# **MOS Capacitors:** Where do the electrons in the inversion layer come from?

#### **Diffusion from the p-type substrate?**

If we relied on diffusion of minority carrier electrons from the p-type substrate it would take a long time to build up the inversion layer charge. The current density of electrons flowing to the interface is just the current across a reverse biased junction (the p-substrate to the inversion layer in this case):  $D_e$ 

$$J_e = q n_i^2 \frac{D_e}{N_A w_{p,eff}} \quad [\text{Coul/cm}^2 - \text{s}]$$

The time,  $\tau$ , it takes this flux to build up an inversion charge is the the increase in the charge,  $\Delta q_n$ , divided by  $J_e$ :

$$\Delta q_N^* = \frac{\varepsilon_{ox}}{t_{ox}} \Delta \left( v_{GB} - V_T \right)$$

so  $\tau$  is

$$\tau = \frac{\Delta q_N^*}{J_e} = \frac{\varepsilon_{ox} N_A w_{p,eff}}{q n_i^2 D_e t_{ox}} \Delta \left( v_{GB} - V_T \right)$$

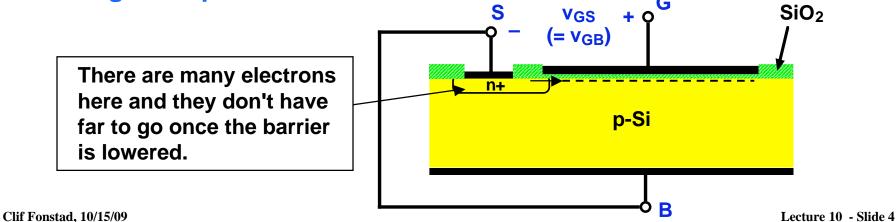
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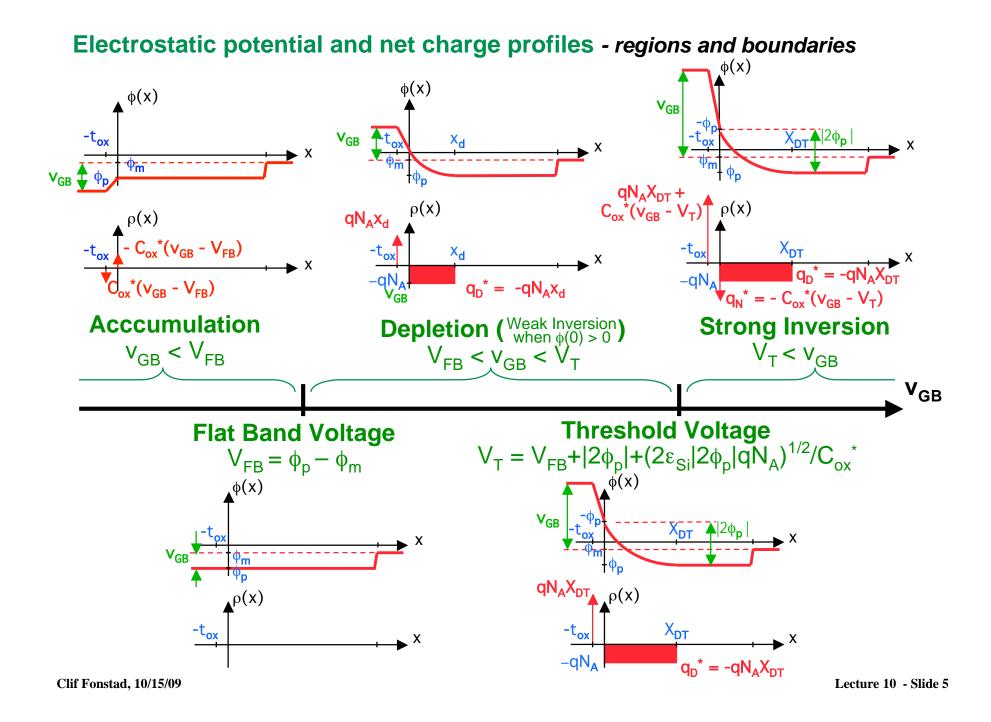
### Diffusion from the p-type substrate. cont.?

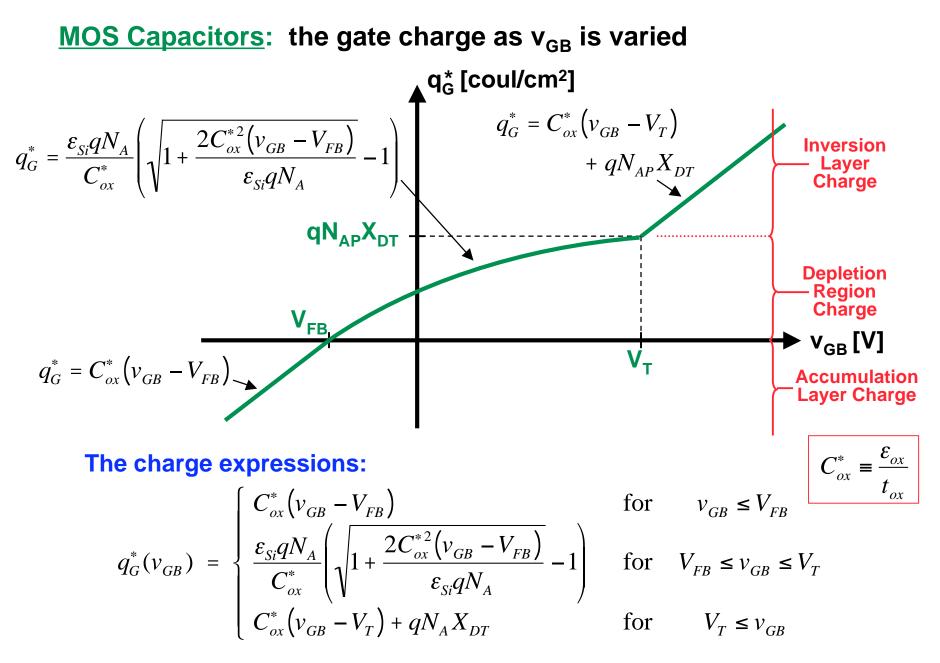
Using N<sub>A</sub> = 10<sup>18</sup> cm<sup>-3</sup>, t<sub>ox</sub> = 3 nm, w<sub>p,eff</sub> = 10 µm, D<sub>e</sub> = 40 cm<sup>2</sup>/V and  $\Delta$ (v<sub>GB</sub>-V<sub>T</sub>) = 0.5 V in the preceding expression for  $\tau$  we find  $\tau \approx 50$  hr!

## Flow from the adjacent n+-region?

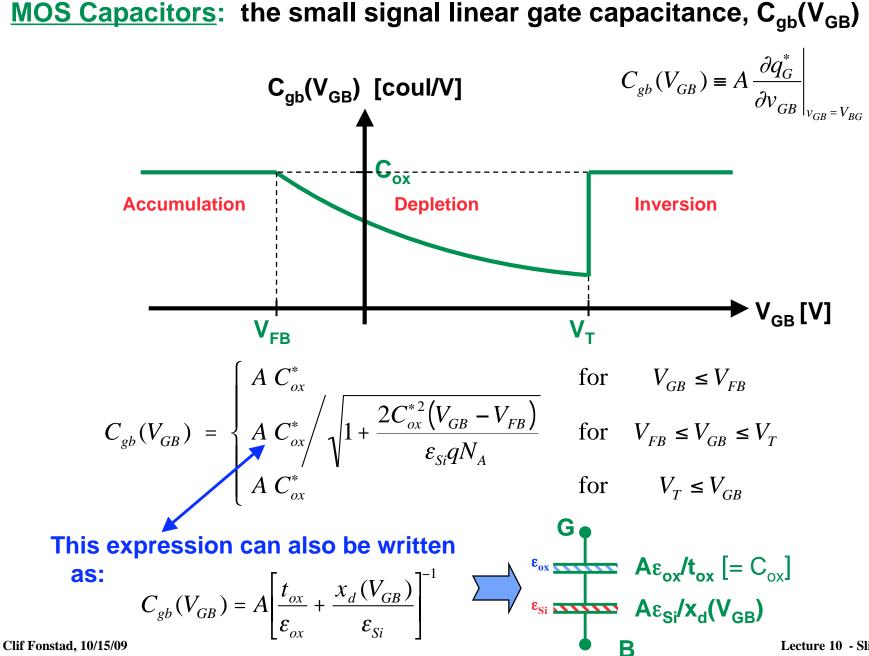
As the surface potential is increased, the potential energy barrier between the adjacent n+ region and the region under the gate is reduced for electrons and they readily flow (diffuse in weak inversion, and drift and diffuse in strong inversion) into the channel; that's why the n+ region is put there:







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## **MOS Capacitors:** How good is all this modeling? How can we know?

#### **Poisson's Equation in MOS**

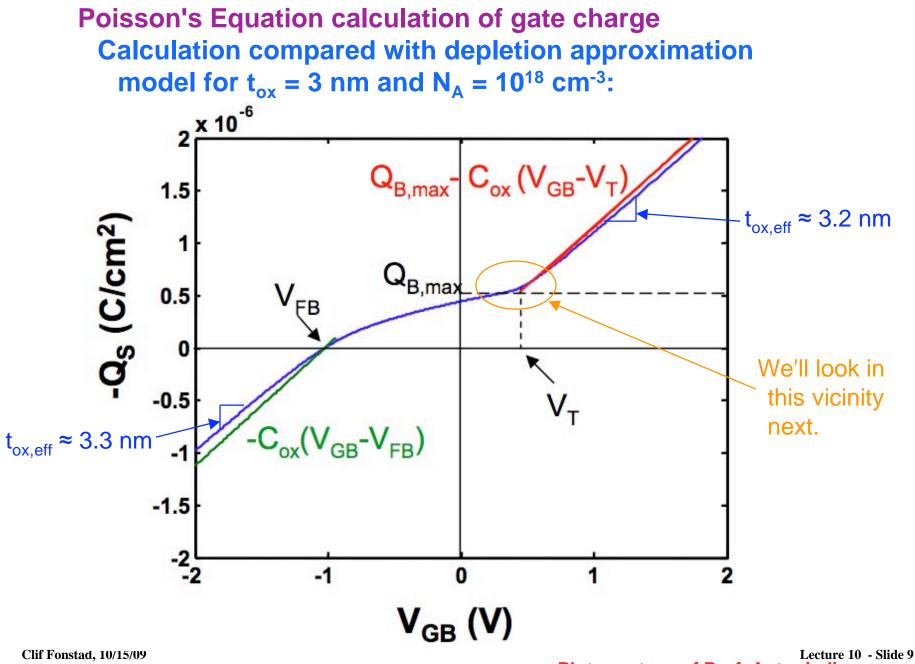
As we argued when starting,  $J_h$  and  $J_e$  are zero in steady state so the carrier populations are in equilibrium with the potential barriers,  $\phi(x)$ , as they are in thermal equilibrium, and we have:

$$n(x) = n_i e^{q\phi(x)/kT}$$
 and  $p(x) = n_i e^{-q\phi(x)/kT}$ 

Once again this means we can find  $\phi(x)$ , and then n(x) and p(x), by solving Poisson's equation:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{q}{\varepsilon} \Big[ n_i \Big( e^{-q\phi(x)/kT} - e^{q\phi(x)/kT} \Big) + N_d(x) - N_a(x) \Big]$$

This version is only valid, however, when  $|\phi(x)| \leq -\phi_p$ . When  $|\phi(x)| > -\phi_p$  we have accumulation and inversion layers, and we assume them to be infinitely thin sheets of charge, i.e. we model them as delta functions.



Plot courtesy of Prof. Antoniadis

## **MOS Capacitors:** Sub-threshold charge Assessing how much we are neglecting

Sheet density of electrons below threshold in weak inversion: In the depletion approximation for the MOS we say that the charge due to the electrons is negligible before we reach threshold and the strong inversion layer builds up:

$$q_{N(inversion)}(v_{GB}) = -C_{ox}^*(v_{GB} - V_T)$$

But how good an approximation is this? To see, we calculate the electron charge below threshold (weak inversion):

$$q_{N(sub-threshold)}(v_{GB}) = -q \int_{x_i(v_{GB})}^0 n_i e^{q\phi(x)/kT} dx$$

This integral is difficult to do because  $\phi(x)$  is non-linear

$$\phi(x) = \phi_p + \frac{qN_A}{2\varepsilon_{Si}} (x - x_d)^2$$

but if we use a linear approximation for  $\phi(x)$  near x = 0, where the term in the integral is largest, we can get a very good approximate analytical expression for the integral.

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### Sub-threshold electron charge, cont. We begin by saying

$$\phi(x) \approx \phi(0) + ax$$
 where  $a \equiv \frac{d\phi(x)}{dx}\Big|_{x=0} = -\sqrt{\frac{2qN_A[\phi(0) - \phi_p]}{\varepsilon_{Si}}}$ 

With this linear approximation to  $\phi(\textbf{x})$  we can do the integral and find

$$q_{N(sub-threshold)}(v_{GB}) \approx q \, \frac{kT}{q} \frac{n(0)}{a} = -q \, \frac{kT}{q} \sqrt{\frac{\varepsilon_{Si}}{2qN_A[\phi(0) - \phi_p]}} \, n_i e^{q\phi(0)/kT}$$

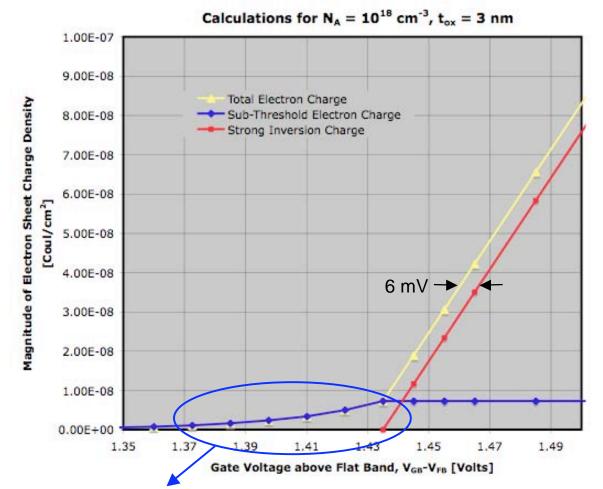
To proceed it is easiest to evaluate this expression for various values of  $\phi(0)$  below threshold (when its value is  $|\phi_p|$ ), and to also find the corresponding value of  $v_{GB}$ , from

$$v_{GB} - V_{FB} = \phi(0) - \phi_p + \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_{Si}qN_A \left[\phi(0) - \phi_p\right]}$$

This has been done and is plotted along with the strong inversion layer charge above threshold on the following foil.

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### Sub-threshold electron charge, cont.



Neglecting this charge results in a 6 mV error in the threshold voltage value, a very minor impact. We will see its impact on sub-threshold MOSFET operation in Lecture 12.

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# MOS Capacitors: A few more questions you might have about our model

- Why does the depletion stop growing above threshold? A positive voltage on the gate must be terminated on negative charge in the semiconductor. Initially the only negative charges are the ionized acceptors, but above threshold the electrons in the strong inversion layer are numerous enough to terminate all the gate voltage in excess of  $V_T$ . The electrostatic potential at 0+ does not increase further and the depletion region stops expanding.
- How wide are the accumulation and strong inversion layers? A parameter that puts a rough upper bound on this is the extrinsic Debye length  $\sqrt{\frac{1}{2}T_{ex}}/\frac{2}{2}N}$

$$L_{eD} \equiv \sqrt{kT\varepsilon_{Si}/q^2}N$$

When N is  $10^{19}$  cm<sup>-3</sup>, L<sub>eD</sub> is 1.25 nm. The figure on Foil 11 seems to say this is ~ 5x too large and that the number is nearer 0.3 nm.\*

Is n, p =  $n_i e^{\pm qV/kT}$  valid in those layers?

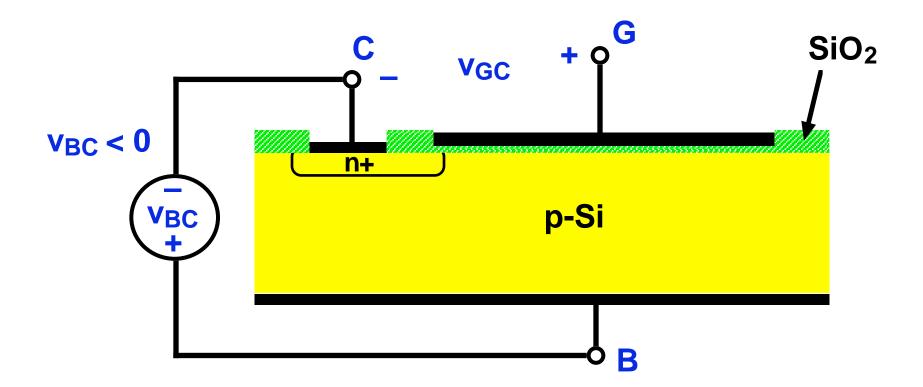
It holds in Si until  $|\phi| \approx 0.54$  V, but when  $|\phi|$  is larger than this Si becomes "degenerate" and the carrier concentration is so large that the simple models we use are no longer sufficient and the dependence on  $\phi$  is more complex. Thinking of degenerate Si as a metal is far easier, and works extremely well for our purposes.

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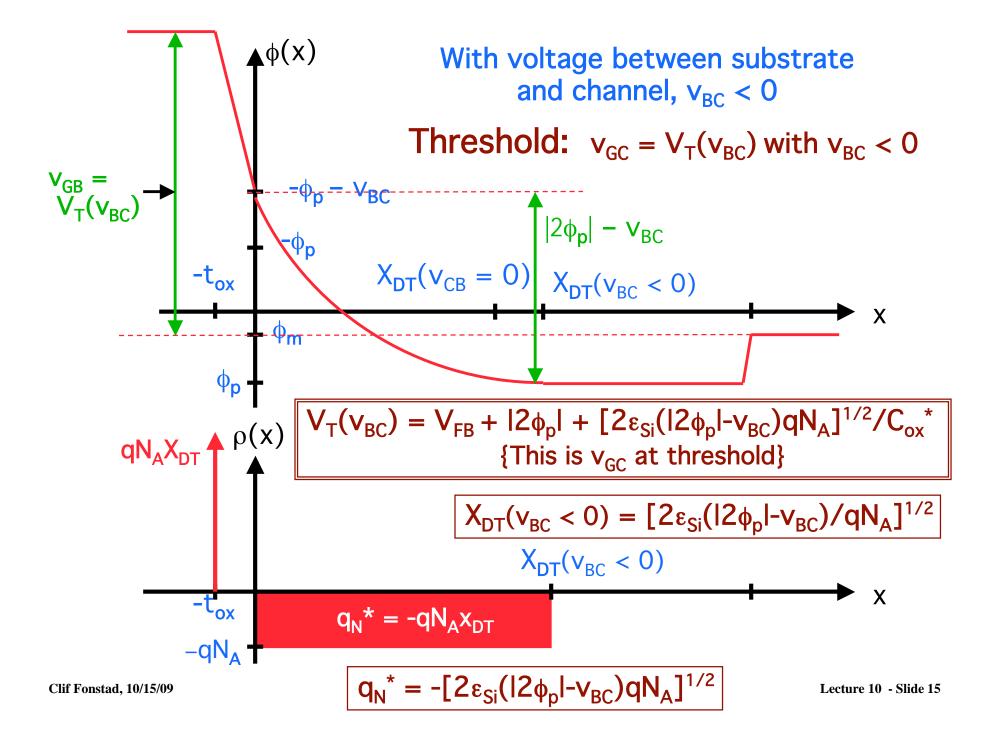
\* Note that when N =  $10^{20}$  cm<sup>-3</sup>, L<sub>eD</sub>  $\approx$  0.4 nm.

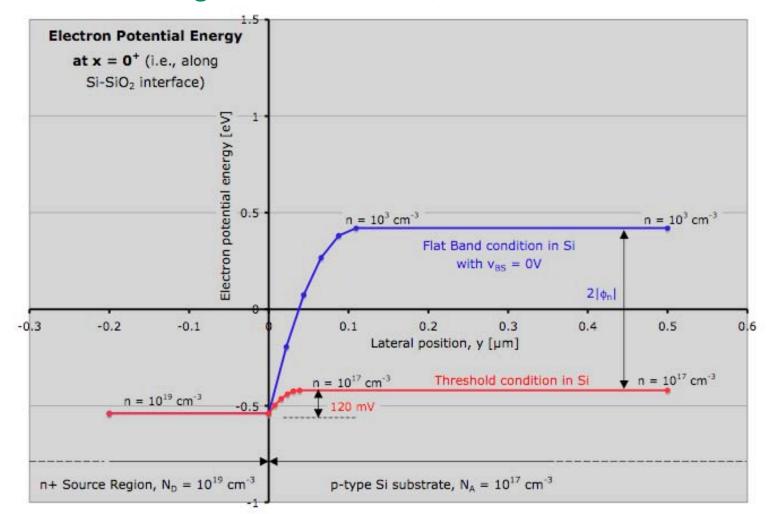
## Bias between n+ region and substrate, cont.

Reverse bias applied to substrate, l.e.  $v_{BC} < 0$ 



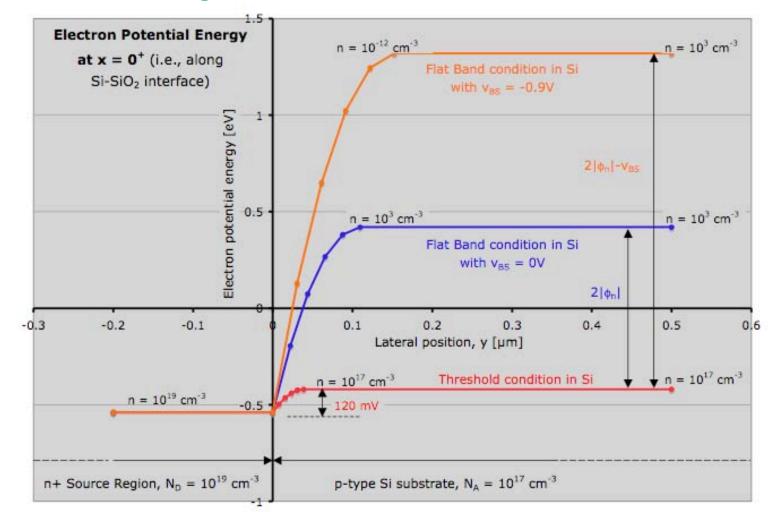
Soon we will see how this will let us electronically adjust MOSFET threshold voltages when it is convenient for us to do so.





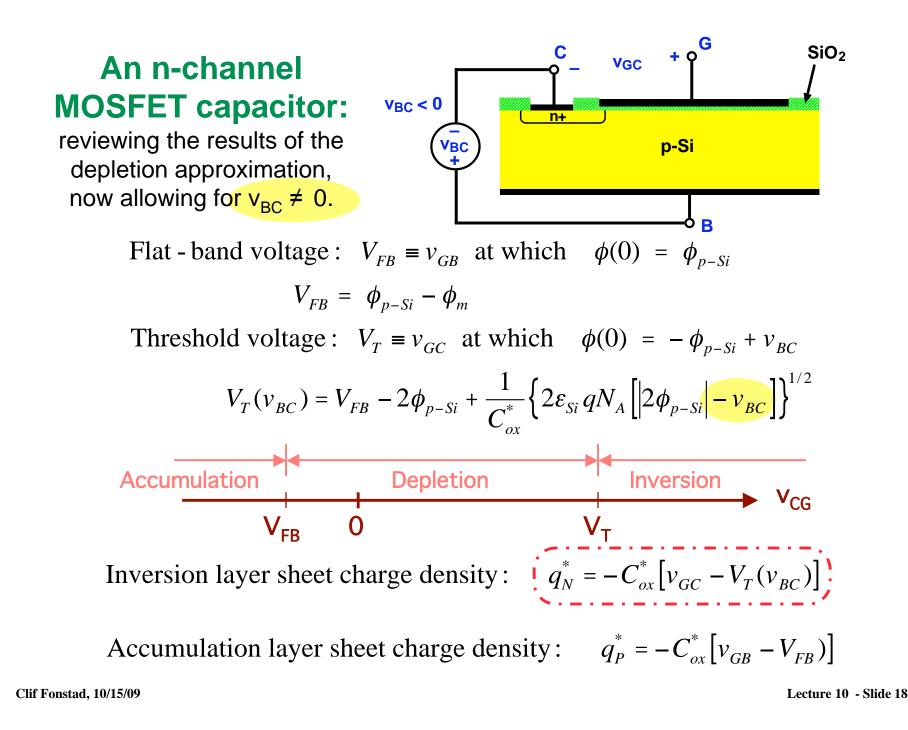
#### Bias between n+ region and substrate, cont. - what electrons see

The barrier confining the electrons to the source is lowered by the voltage on the gate, until high level injection occurs at threshold.

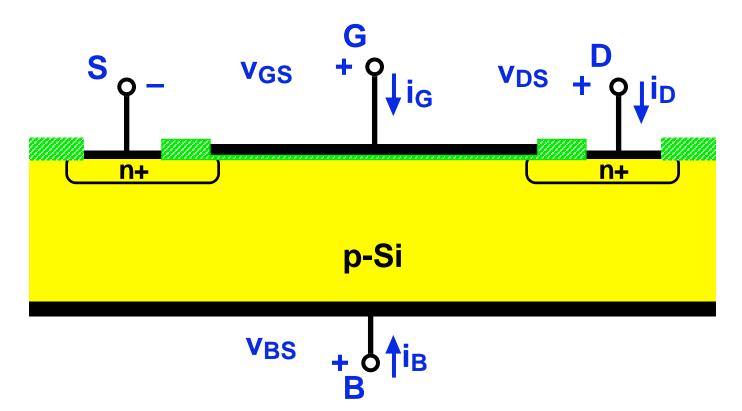


#### Bias between n+ region and substrate, cont. - what electrons see

The barrier confining the electrons to the source is lowered by the voltage on the gate, until high level injection occurs at threshold. When the source-substrate junction is reverse biased, the barrier is higher, and the gate voltage needed to reach threshold is larger. Clif Fonstad, 10/15/09

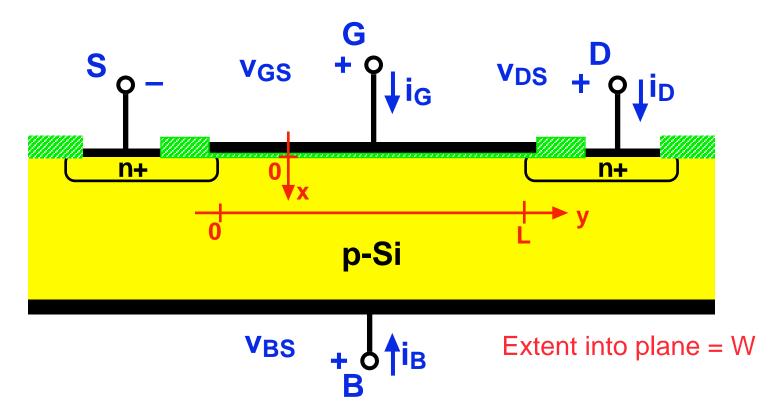


# **An n-channel MOSFET**



<u>**Gradual Channel Approximation:**</u> There are two parts to the problem: the <u>vertical electrostatics problem</u> of relating the channel charge to the voltages, and the <u>horizontal drift problem</u> in the channel of relating the channel charge drift to the voltages. We will assume they can be worked independently and in sequence.

# An n-channel MOSFET showing gradual channel axes



## **Gradual Channel Approximation:**

- We first solve a <u>one-dimensional electrostatics problem</u> in the x direction to find the channel charge, q<sub>N</sub><sup>\*</sup>(y)
- Then we solve a <u>one-dimensional drift problem</u> in the y direction to find the channel current,  $i_D$ , as a function of  $v_{GS}$ ,  $v_{DS}$ , and  $v_{BS}$ .

# **Gradual Channel Approximation i-v Modeling**

(n-channel MOS used as the example)

We restrict voltages to the following ranges:

 $v_{\scriptscriptstyle BS} \leq 0, \ v_{\scriptscriptstyle DS} \geq 0$ 

This means that the source-substrate and drain-substrate junctions are always reverse biased and thus that:

$$i_B(v_{GS}, v_{DS}, v_{BS}) \approx 0$$

The gate oxide is insulating so we also have:

$$i_G(v_{GS}, v_{DS}, v_{BS}) \approx 0$$

With the back current,  $i_B$ , zero, and the gate current,  $i_G$ , zero, the only current that is not trivial to model is  $i_D$ . The drain current,  $i_D$ , is also zero except when when  $v_{GS} > V_T$ .

The <u>in-plane</u> problem: (for just a minute so we can see where we're going) Looking at electron drift in the channel we write i<sub>D</sub> as

 $i_D = -W s_{ey}(y) q_n^*(y) = -W \mu_e q_n^*(v_{GS}, v_{BS}, v_{CS}(y)) \frac{dv_{cs}}{dy}$ (at moderate E - fields)

This can be integrated from y = 0 to y = L, and  $v_{CS} = 0$  to  $v_{CS} = v_{DS}$ , to get  $i_D(v_{GS}, v_{DS}, v_{BS})$ , but first we need  $q_n(y)$ .

We get  $q_n^*(y)$  from the normal problem, which we do next.

The <u>normal</u> problem:

The channel charge at y is  $q_n^*(y)$ , which is:

$$q_{n}^{*}(y) = -C_{ox}^{*} \{ v_{GC}(y) - V_{T}[v_{CS}(y), v_{BS}] \} = -C_{ox}^{*} \{ v_{GS} - v_{CS}(y) - V_{T}[v_{CS}(y), v_{BS}] \}$$
  
with  $V_{T}[v_{CS}(y), v_{BS}] = V_{FB} - 2\phi_{p-Si} + \{ 2\varepsilon_{Si}qN_{A}[|2\phi_{p-Si}| - v_{BS} + v_{CS}(y)] \}^{1/2} / C_{ox}^{*}$ 

We <u>can</u> substitute this expression into the i<sub>D</sub> equation we just had and integrate it, but the resulting expression is deemed too algebraically awkward:

$$i_{D}(v_{DS}, v_{GS}, v_{BS}) = \frac{W}{L} \mu_{e} C_{ox}^{*} \left\{ \left( \frac{v_{GS} - |2\phi_{p}| - v_{FB} - \frac{v_{DS}}{2} \right) + \frac{3}{2} \sqrt{2\varepsilon_{si}qN_{A}} \left[ \left( |2\phi_{p}| + v_{DS} - v_{BS} \right)^{3/2} - \left( |2\phi_{p}| - v_{BS} \right)^{3/2} \right] \right\}$$

A simpler, more common approach is to simply ignore the dependence of  $V_T$  on  $v_{CS}$ , and thus to say

$$V_{T}[v_{CS}(y), v_{BS}] \approx V_{T}(v_{BS}) = V_{FB} - 2\phi_{p-Si} + \left\{ 2\varepsilon_{Si}qN_{A} \left[ \left| 2\phi_{p-Si} \right| - v_{BS} \right] \right\}^{1/2} / C_{ox}^{*}$$

With this simplification we have:

$$q_n^*(y) \approx -C_{ox}^* [v_{GS} - V_T(v_{BS}) - v_{CS}(y)]$$

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(derivation continues on next foil)

The drain current expression (the in-plane problem):

Putting our approximate expression for the channel charge into the drain current expression we obtained from considering the in-plane problem, we find:

$$i_{D} = -W \mu_{e} q_{n}^{*}(v_{CS}) \frac{dv_{CS}}{dy} \approx W \mu_{e} C_{ox}^{*} \{v_{GS} - V_{T}(v_{BS}) - v_{CS}(y)\} \frac{dv_{CS}}{dy}$$

This expression can be integrated with respect to dy for y = 0 to y = L. On the left-hand the integral with respect to y can be converted to one with respect to  $v_{CS}$ , which ranges from 0 at y = 0, to  $v_{DS}$  at y = L:

$$\int_{0}^{L} i_{D} \, dy = \int_{0}^{v_{DS}} W \, \mu_{e} \, C_{ox}^{*} \{ v_{GS} - V_{T}(v_{BS}) - v_{CS}(y) \} \, dv_{CS}$$

Doing the definite integrals on each side we obtain a relatively simple expression for i<sub>D</sub>:

$$i_D L = W \mu_e C_{ox}^* \left\{ v_{GS} - V_T(v_{BS}) - \frac{v_{DS}}{2} \right\} v_{DS}$$

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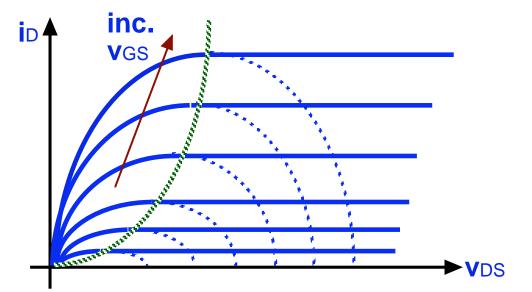
(derivation continues on next foil)

The drain current expression, cont:

Isolating the drain current, we have, finally:

$$i_D(v_{GS}, v_{DS}, v_{BS}) = \frac{W}{L} \mu_e C_{ox}^* \left[ v_{GS} - V_T(v_{BS}) - \frac{v_{DS}}{2} \right] v_{DS}$$

Plotting this equation for increasing values of  $v_{GS}$  we see that it traces inverted parabolas as shown below.



Note, however, that  $i_D$  <u>saturates</u> at its peak value for larger values of  $v_{DS}$  (solid lines); it doesn't fall off (dashed lines).

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The drain current expression, cont:

The point at which i<sub>D</sub> reaches its peak value and saturates is<br/>easily found. Taking the derivative and setting it equal to<br/>zero we find: $\frac{\partial i_D}{\partial v_{DS}} = 0$  when  $v_{DS} = [v_{GS} - V_T(v_{BS})]$ 

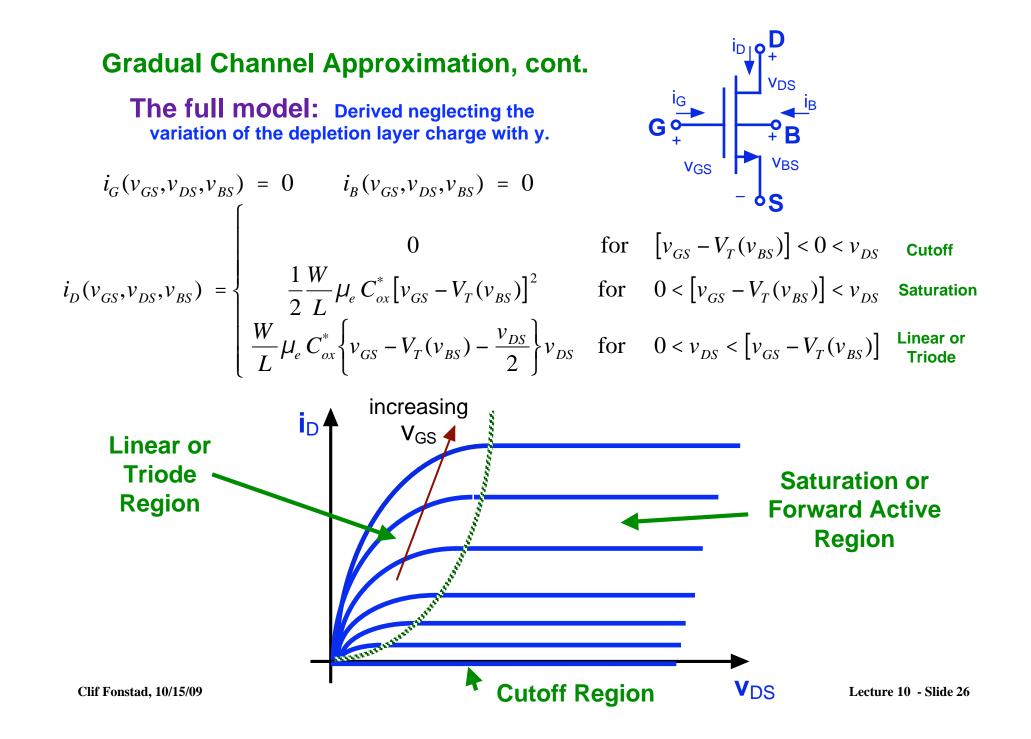
What happens physically at this voltage is that the channel (inversion) at the drain end of the channel disappears:

$$q_n^*(L) \approx -C_{ox}^* \{ v_{GS} - V_T(v_{BS}) - v_{DS} \}$$
  
= 0 when  $v_{DS} = [v_{GS} - V_T(v_{BS})]$ 

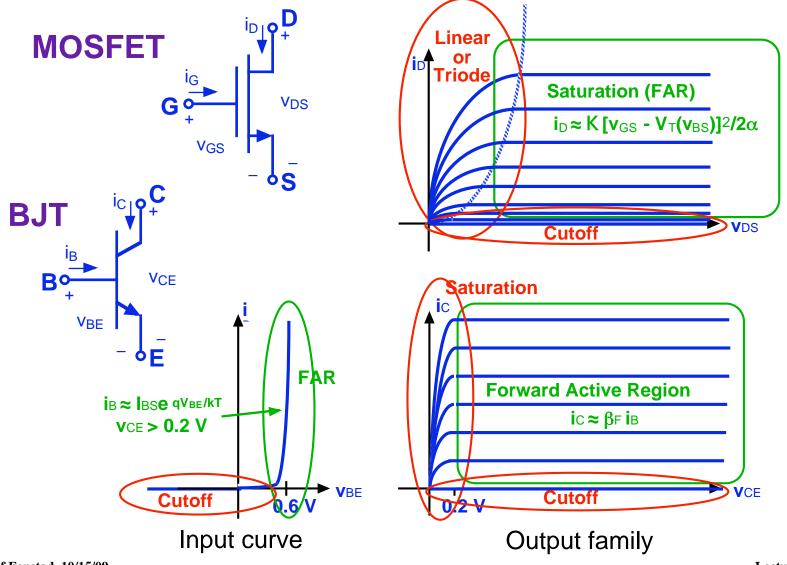
For  $v_{DS} > [v_{GS}-V_T(v_{BS})]$ , all the additional drain-to-source voltage appears across the high resistance region at the drain end of the channel where the mobile charge density is very small, and  $i_D$  remains constant independent of  $v_{DS}$ :

$$i_{D}(v_{GS}, v_{DS}, v_{BS}) = \frac{1}{2} \frac{W}{L} \mu_{e} C_{ox}^{*} [v_{GS} - V_{T}(v_{BS})]^{2} \text{ for } v_{DS} > [v_{GS} - V_{T}(v_{BS})]$$

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## The operating regions of MOSFETs and BJTs: Comparing an n-channel MOSFET and an npn BJT



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# 6.012 - Microelectronic Devices and Circuits Lecture 10 - MOS Caps II; MOSFETs I - Summary

# • Quantitative modeling (Apply depl. approx. to MOS cap., $v_{BC} = 0$ )

**Definitions:**  $V_{FB} \equiv v_{GB}$  such that  $\phi(0) = \phi_{p-Si}$   $C_{ox}^* \equiv \varepsilon_{ox}/t_{ox}$ 

$$V_{T} \equiv V_{GB}$$
 such that  $\phi(0) = -\phi_{p-Si}$ 

#### **Results and expressions** (For n-MOS example)

- 1. Flat-band voltage,  $V_{FB}=\varphi_{p\text{-}Si}-\varphi_m$
- 2. Accumulation layer sheet charge density,  $q_{A^*} = -C_{ox^*}(v_{GB} V_{FB})$
- 3. Maximum depletion region width,  $X_{DT} = [2\epsilon_{Si}|2\phi_{p-Si}|/qN_A]^{1/2}$
- 4. Threshold voltage,  $V_T = V_{FB} 2\phi_{p-Si} + [2\epsilon_{Si} q N_A | 2\phi_{p-Si} |]^{1/2} / C_{ox}^*$

5. Inversion layer sheet charge density,  $q_{N^*} = -C_{ox^*}(v_{GB} - V_T)$ 

# Subthreshold charge

**Negligible?:** Yes in general, but (1) useful in some cases, and (2) an issue for modern ULSI logic and memory circuits

## • MOS with bias applied to the adjacent n<sup>+</sup>-region Maximum depletion region width: $X_{DT} = [2\epsilon_{Si}(|2\phi_{p-Si}| - v_{BC})/qN_A]^{1/2}$ Threshold voltage: $V_T = V_{FB} - 2\phi_{p-Si} + [2\epsilon_{Si}qN_A(|2\phi_{p-Si}| - v_{BC})]^{1/2}/C_{ox}^*$

• MOSFET i-V (the Gradual Channel Approximation) (v<sub>gc</sub> at threshold) Vertical problem for channel charge; in-plane drift to get current 6.012 Microelectronic Devices and Circuits Fall 2009

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