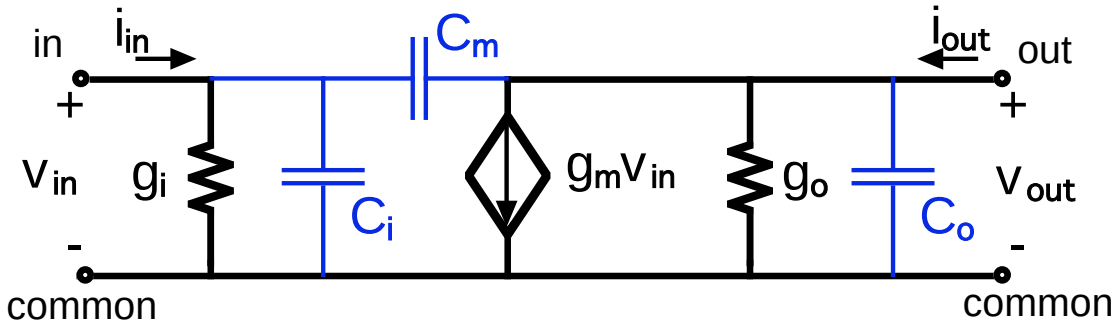
Lecture 14 - Digital Circuits: Inverter Basics - Outline

- **Announcements**
  - Stellar - Two supplemental readings posted
  - Exam Two - Be the first in your living unit to study for it.
- **Review - Linear Equivalent Circuits**
  - Everything depends on the bias; only low frequency for now
- **Digital building blocks - inverters**
  - A generic inverter
  - MOS inverter options
- **Digital inverter performance metrics**
  - Transfer characteristic: logic levels and noise margins
  - Power dissipation
  - Switching speed
  - Fan-out, fan-in
  - Manufacturability
- **Comparing the MOS options**
  - And the winner is….

Reviewing our LECs: Important points made in Lec. 14

We found LECs for BJTs and MOSFETs in both strong inversion and sub-threshold. When $v_{bs} = 0$, they all look very similar:



Most linear circuits are designed to operate at frequencies where the capacitors look like open circuits. We can thus do our designs neglecting them.*

Bias dependences:

	BJT	ST MOS	SI MOS
g_i :	$qI_C/\beta_F kT$	0	0
g_m :	qI_C/kT	$qI_D/n\,kT$	$\sqrt{2K_o I_D/\alpha}$
g_o :	λI_C	λI_D	λI_D

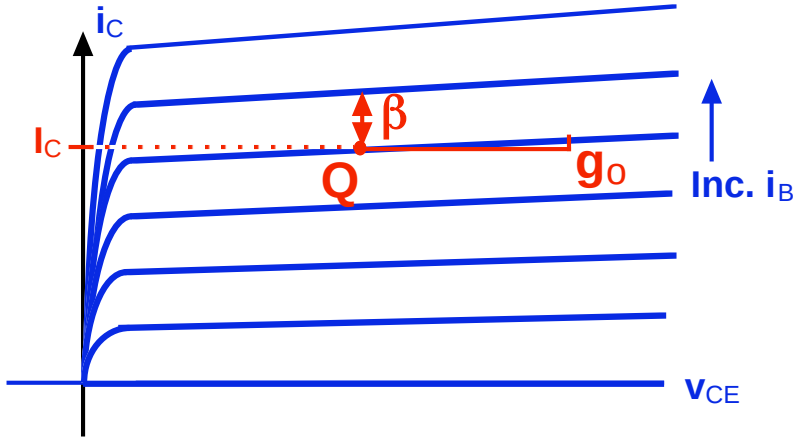
ST = sub-threshold
SI = strong inversion

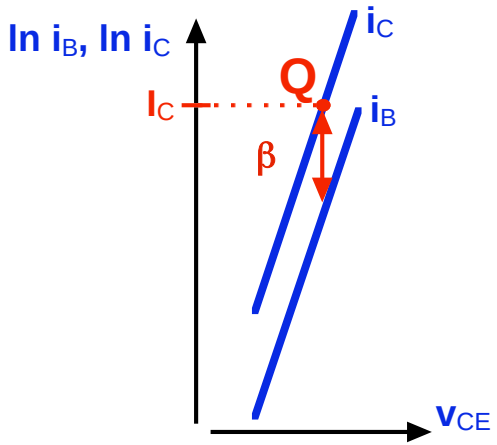
The LEC elements all depend on the bias levels. Establishing a known, stable bias point is a key part of linear circuit design. We use our large signal models in this design and analysis.

* Only when we want to determine the maximum frequency to which our designs can usefully operate must we include the capacitors.

LECs: Identifying the incremental parameters in the characteristics

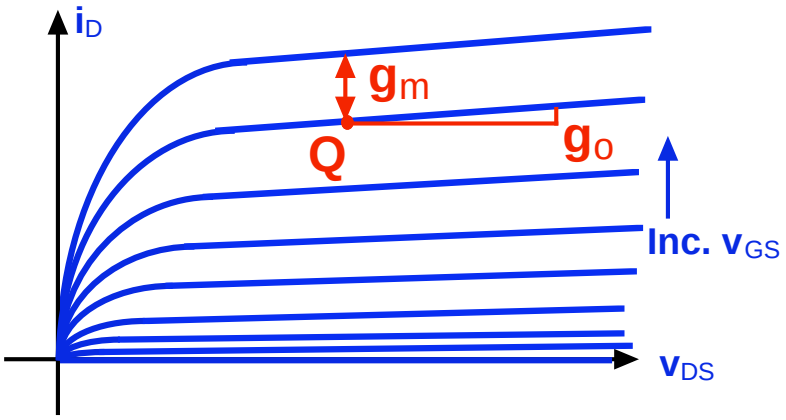
BJT:

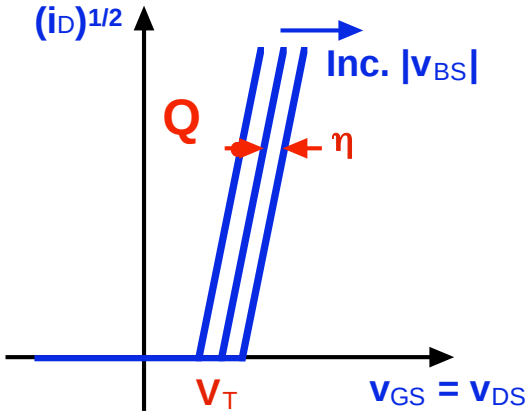




$g_m = qI_C/kT$; $g_\pi = \beta g_m$ with $\beta = di_C/di_B|_Q$; $g_o = di_C/dv_{CE}|_Q$

MOSFET:



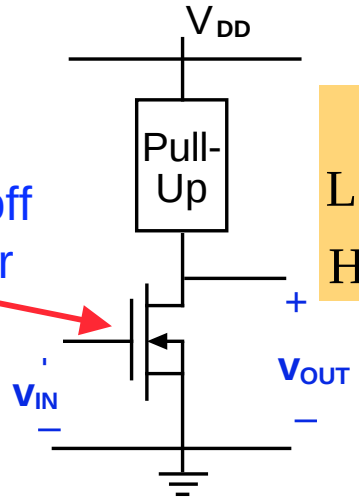


$g_m = di_D/dv_{GS}|_Q$; $g_{mb} = \eta g_m$ with $\eta = -dV_T/dv_{BS}|_Q$; $g_o = di_D/dv_{DS}|_Q$

Building Blocks for Digital Circuits: inverters

A basic inverter

Device: on or off
Switch: open or closed



v_{IN}	v_{OUT}
Lo (0)	Hi (1)
Hi (1)	Lo (0)

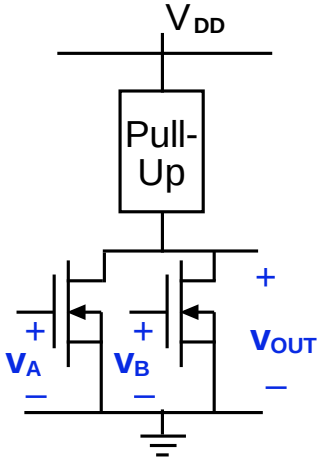
Performance metrics

- Transfer characteristic
- Logic levels
- Noise margins
- Power dissipation
- Switching speed
- Fan-in/Fan-out
- Manufacturability

Logic gates

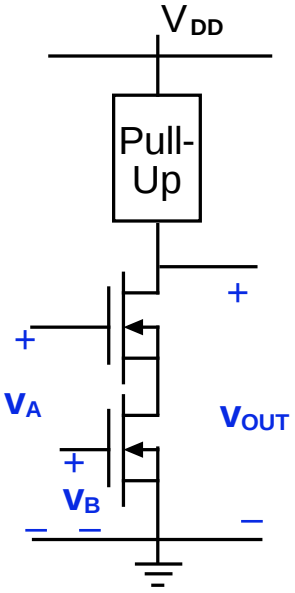
NOR:

v_A	v_B	v_{OUT}
0	0	1
0	1	0
1	0	0
1	1	0

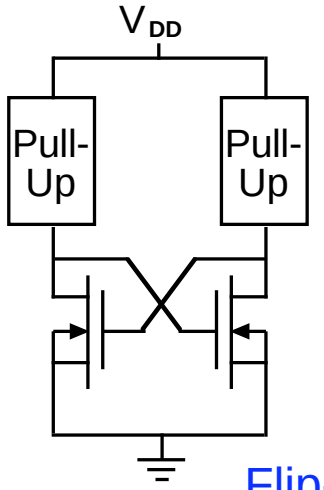


NAND:

v_A	v_B	v_{OUT}
0	0	1
0	1	1
1	0	1
1	1	0



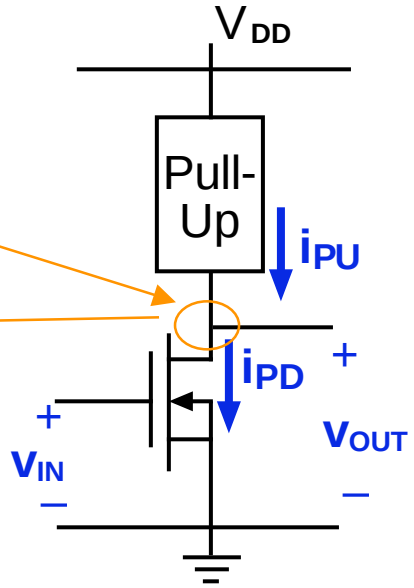
Memory cell



Flip-flop

Inverter metrics: Transfer characteristic

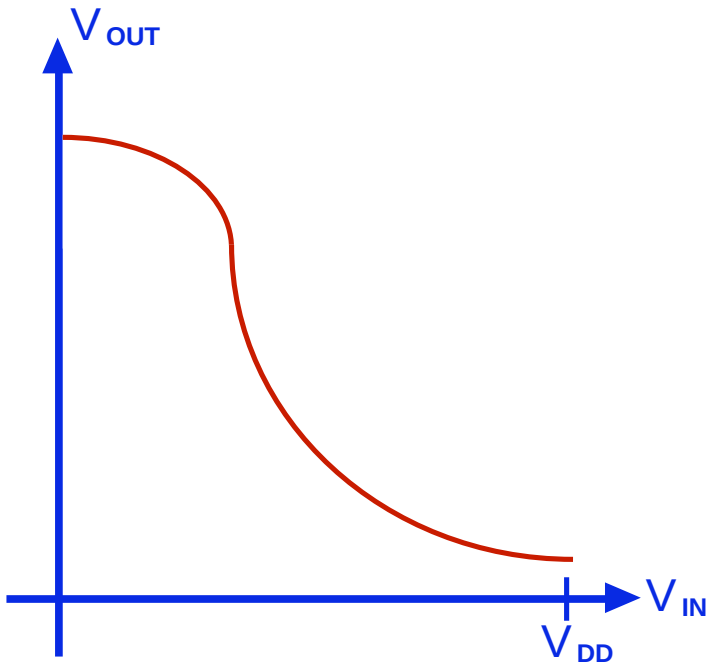
The transfer characteristic, v_{OUT} vs v_{IN}, is found applying the large signal models at this node



Node equation: $i_{PD} = i_{PU}$

$$i_{PD} = \begin{cases} 0^{*} \\ \quad \text{when} \quad v_{IN} < V_{T,PD} \\ K_{PD}\left(v_{IN} - V_{T,PD}\right)^2 / 2 \\ \quad \text{when} \quad 0 < \left[v_{IN} - V_{T,PD}\right] < v_{OUT} \\ K_{PD}\left(v_{IN} - V_{T,PD} - v_{OUT}/2\right)v_{OUT} \\ \quad \text{when} \quad 0 < v_{OUT} < \left[v_{IN} - V_{T,PD}\right] \end{cases}$$

i_{PU} : Depends on the specific pull-up device used.



For simplicity: $\alpha = 1$, $\lambda = 0$

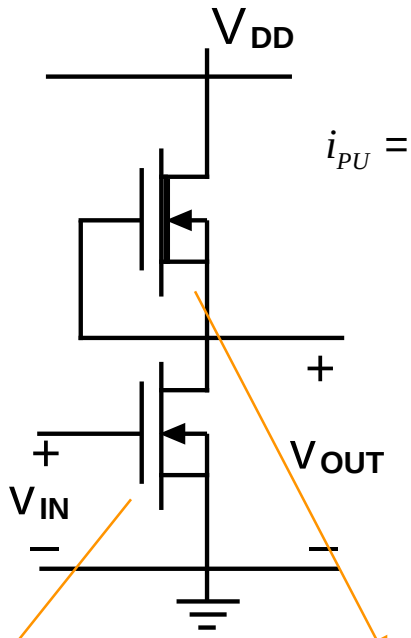
*** Note: We can say i_{PD} is zero for the purpose of calculating a transfer characteristic. For power we may want to use:** $i_{PD,off} = I_{S,s-t}e^{-V_T/nV_t}$

Inverter metrics: Transfer characteristic, cont.

An example: NMOS

Pull-up: Depletion mode n-channel MOSFET
(Note: $V_{T,PU} < 0$)

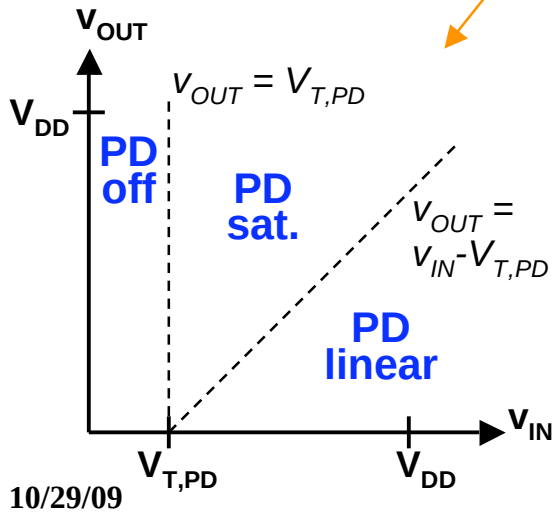
Pull-down: Enhancement mode n-channel MOSFET

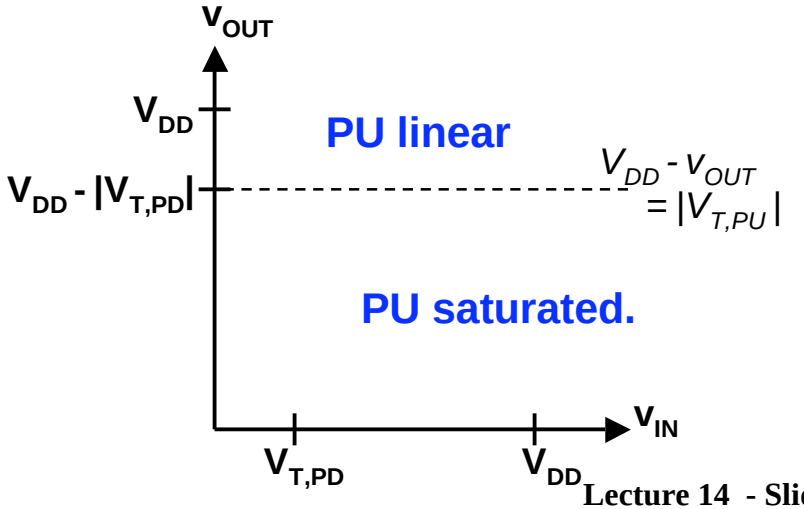


$$i_{PU} = \begin{cases} K_{PU}\left|V_{T,PU}\right|^2/2 \\ \quad \text{when} \quad 0 < \left|V_{T,PU}\right| < \left[V_{DD} - v_{OUT}\right] \\ K_{PU}\left[\left|V_{T,PU}\right| - \left(V_{DD} - v_{OUT}\right)/2\right]\left(V_{DD} - v_{OUT}\right) \\ \quad \text{when} \quad 0 < \left[V_{DD} - v_{OUT}\right] < \left|V_{T,PU}\right| \end{cases}$$

$$i_{PD} = \begin{cases} 0 \\ \quad \text{when} \quad v_{IN} < V_{T,PD} \\ K_{PD}\left(v_{IN} - V_{T,PD}\right)^2/2 \\ \quad \text{when} \quad 0 < \left[v_{IN} - V_{T,PD}\right] < v_{OUT} \\ K_{PD}\left(v_{IN} - V_{T,PD} - v_{OUT}/2\right)v_{OUT} \\ \quad \text{when} \quad 0 < v_{OUT} < \left[v_{IN} - V_{T,PD}\right] \end{cases}$$

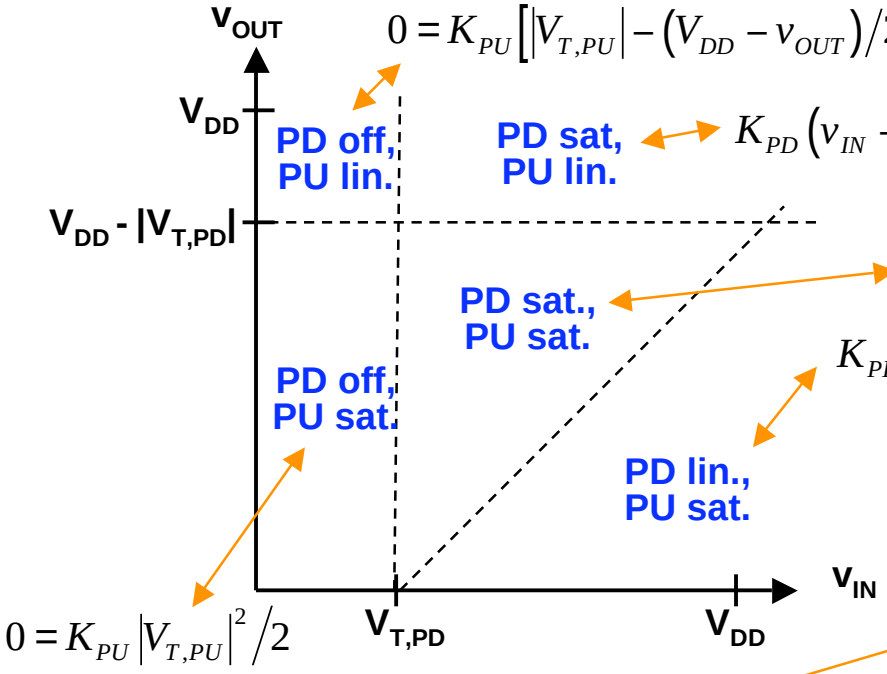
Identify the regions





Inverter metrics: Transfer characteristic, cont.

Combine the plots; write the node equation in each region and solve.



$$0 = K_{PU}\left[|V_{T,PU}| - (V_{DD} - v_{OUT})/2\right](V_{DD} - v_{OUT})$$

$$K_{PD}\left(v_{IN} - V_{T,PD}\right)^2/2 = K_{PU}\left[|V_{T,PU}| - (V_{DD} - v_{OUT})/2\right](V_{DD} - v_{OUT})$$

$$K_{PD}\left(v_{IN} - V_{T,PD}\right)^2/2 = K_{PU}|V_{T,PU}|^2/2$$

$$K_{PD}\left(v_{IN} - V_{T,PD} - v_{OUT}/2\right)v_{OUT} = K_{PU}|V_{T,PU}|^2/2$$

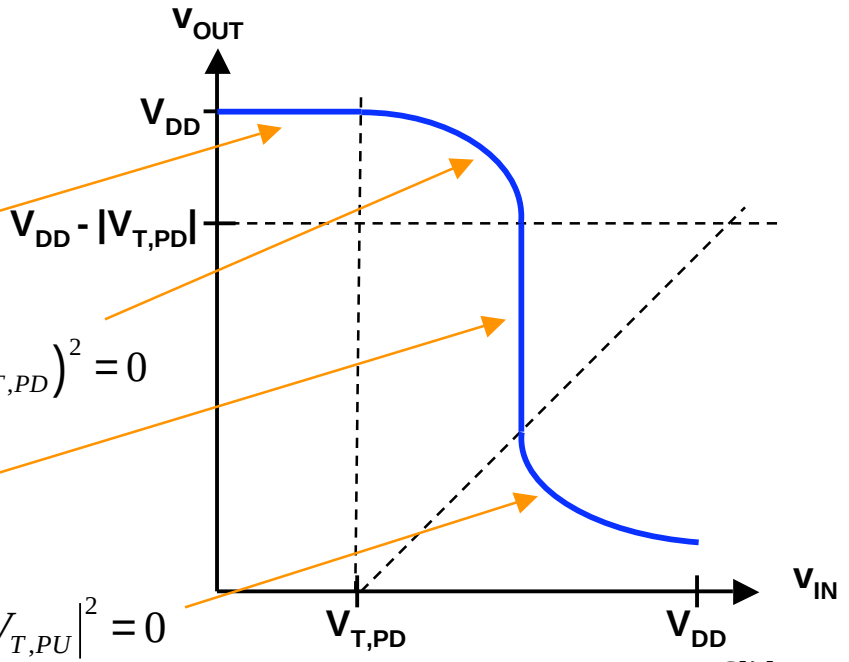
$$0 = K_{PU}|V_{T,PU}|^2/2$$

$$v_{OUT} = V_{DD}$$

$$\left(V_{DD} - v_{OUT}\right)^2 - 2|V_{T,PU}|(V_{DD} - v_{OUT}) + \frac{K_{PD}}{K_{PU}}\left(v_{IN} - V_{T,PD}\right)^2 = 0$$

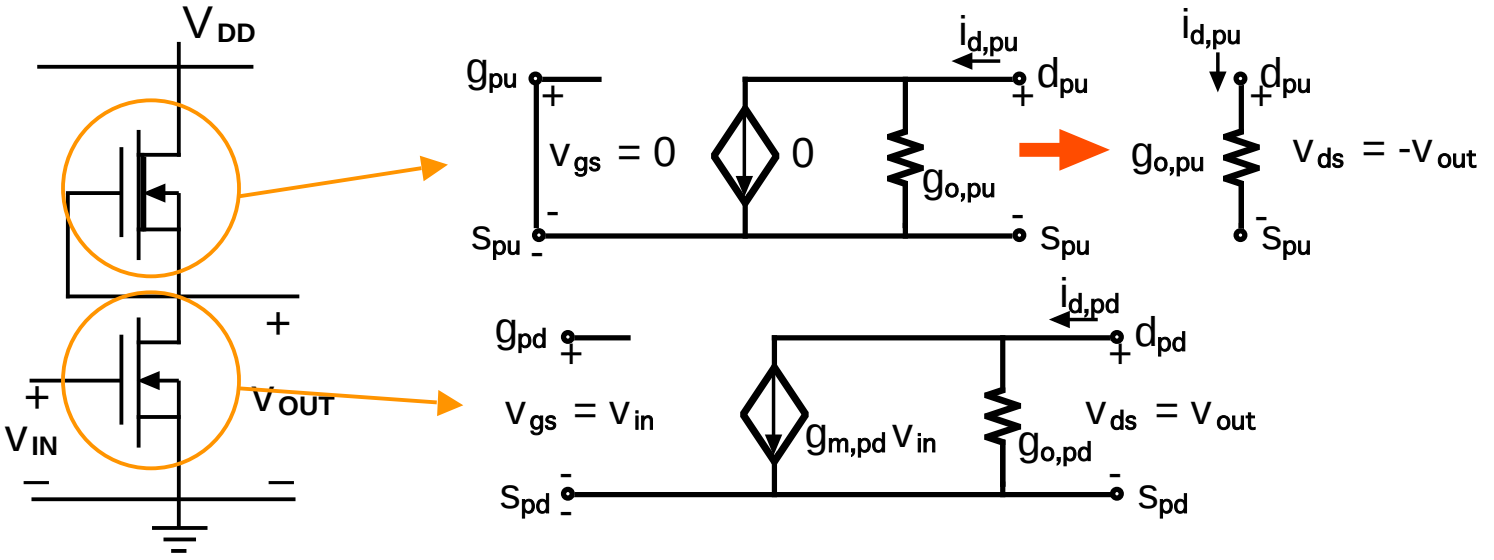
$$v_{IN} = \sqrt{\frac{K_{PU}}{K_{PD}}}\left(V_{T,PD} + |V_{T,PU}|\right)$$

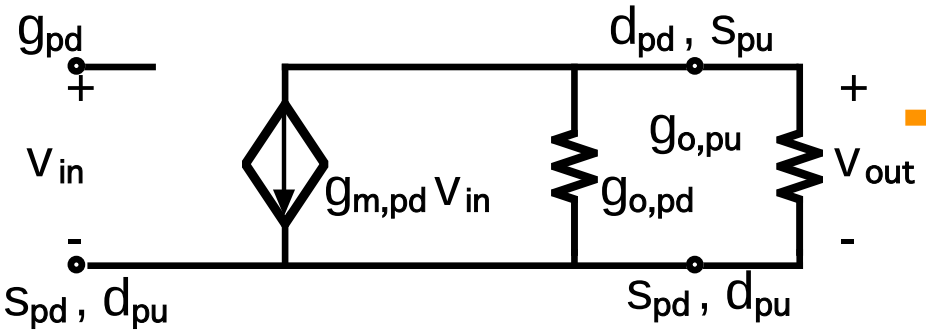
$$v_{OUT}^2 - 2\left(v_{IN} - V_{T,PD}\right)v_{OUT} - \frac{K_{PU}}{K_{PD}}|V_{T,PU}|^2 = 0$$



Inverter metrics: Transfer characteristic, cont.

Is the characteristic really vertical and v_{OUT} indeterminate when both transistors are in saturation? It is if $\lambda = 0$ (i.e. no Early effect), but we know this isn't true. We can find the slope when $\lambda \neq 0$ from an LEC analysis about the bias point $v_{OUT} = v_{IN} = \sqrt{K_{PU}/K_{PD}}\left(V_{T,PD} + |V_{T,PU}|\right)$.





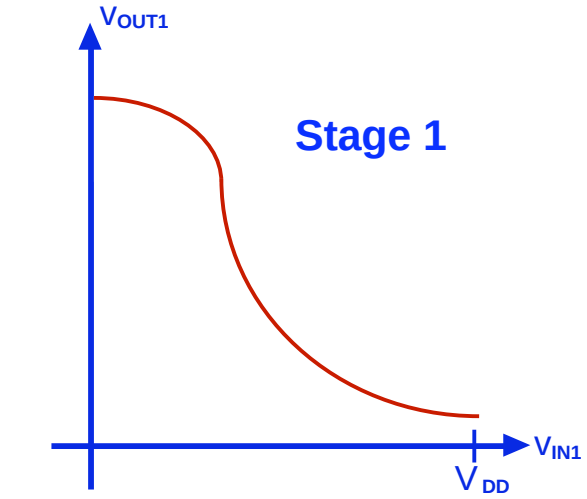
$$A_v \equiv \frac{v_{out}}{v_{in}} = -\frac{g_{m,pd}}{g_{o,pd} + g_{o,pu}}$$

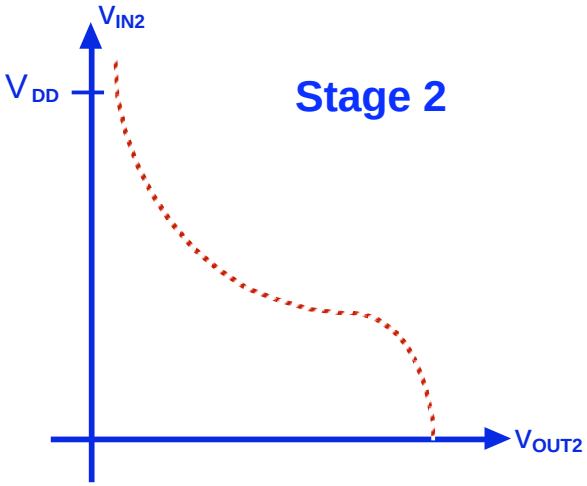
$$= -\frac{\sqrt{2K_{PD}I_D}}{\lambda_{PD}I_D + \lambda_{PU}I_D}$$

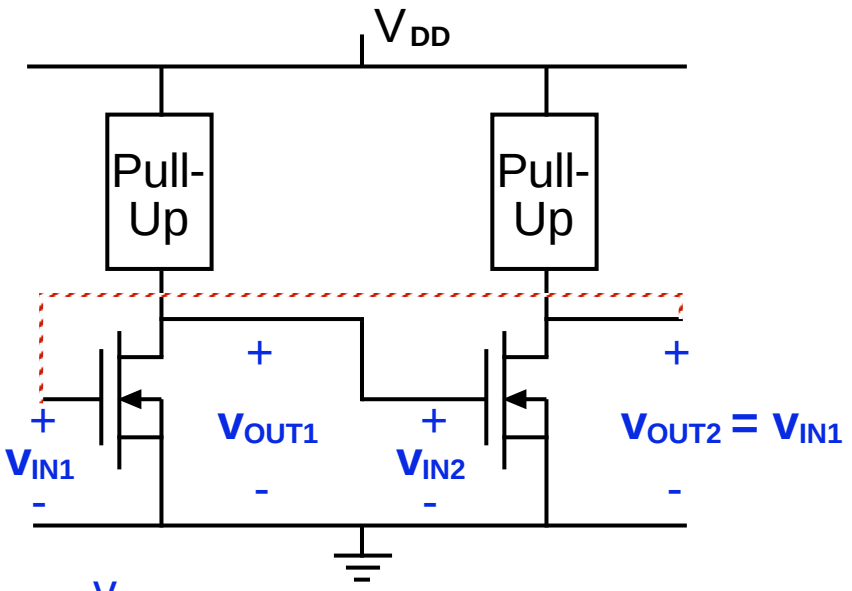
This is the slope of the "vertical" portion.

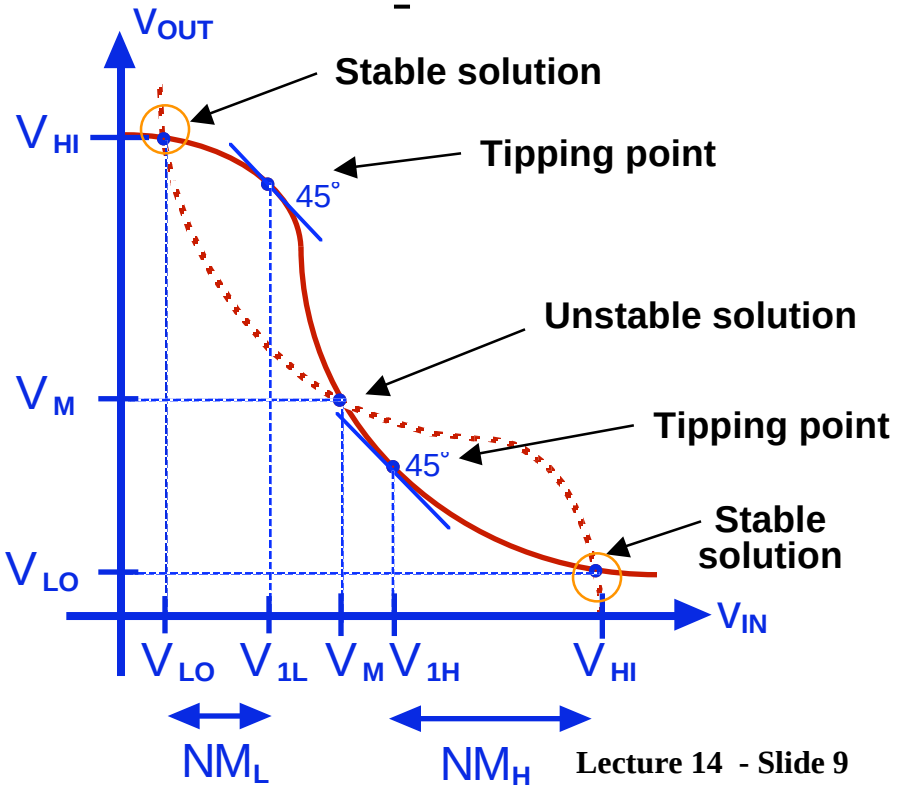
Inverter metrics:

Logic levels, noise margins



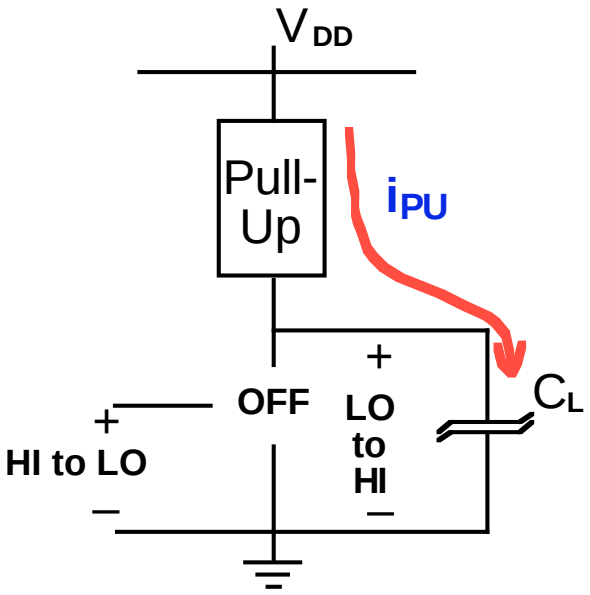


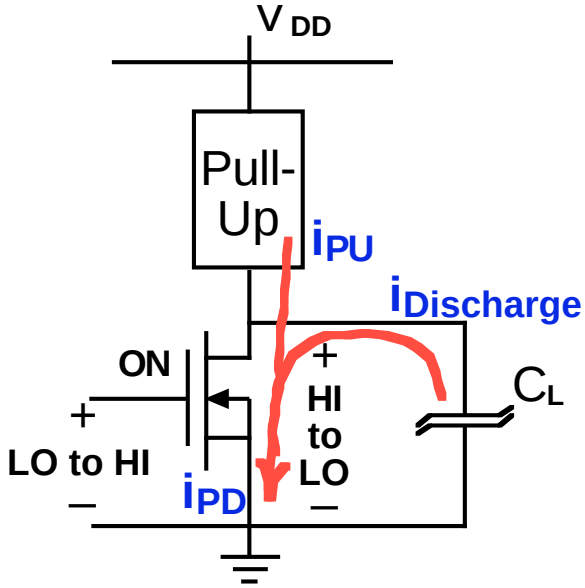




Inverter metrics: Switching times (gate delay)

When the output goes from LO to HI, the load charge store must be charged through the pull-up device. When the output goes from HI to LO, it is discharged through the pull-down device.





Charging cycle: $i_{Charge} = i_{PU}$ **Discharging cycle:** $i_{Discharge} = i_{PD} - i_{PU}$

We can often model C_L as a linear capacitor (i.e. a multiple of C_{ox}*) in which case the charge and discharge cycles are found by solving:

$$\tau_{Charge}: \frac{dv_{OUT}}{dt} = \frac{1}{C_L} i_{PU}(v_{OUT}) \qquad \tau_{Discharge}: \frac{dv_{OUT}}{dt} = \frac{1}{C_L}\left[i_{PD}(v_{IN}, v_{OUT}) - i_{PU}(v_{OUT})\right]$$

Inverter metrics: Power

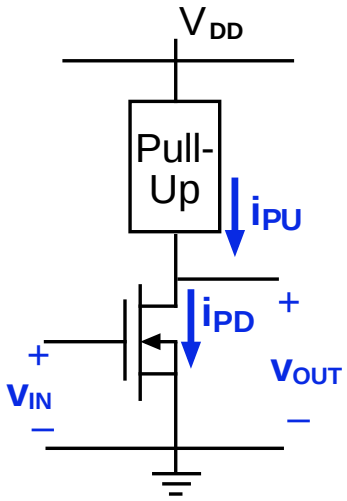
Total Power:

Two components - static and dynamic (switching)

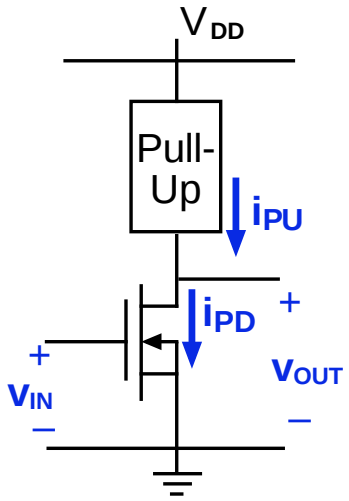
$$P_{Total} = P_{Static} + P_{Dynamic}$$

Static:

Pull-down off:



Pull-down on:



$$P_{Static,off} = I_{PD,off} V_{DD} \quad (\approx 0)$$

$$P_{Static,on} = I_{PU,on} V_{DD}$$

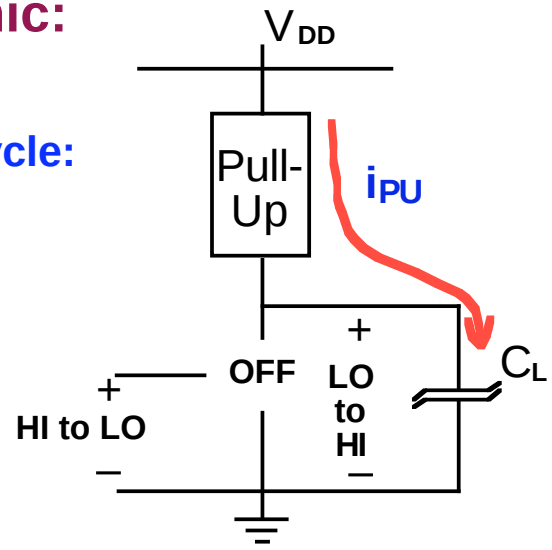
To estimate the total static power we assume the typical pull-down is off half the time and on half the time.

$$P_{Static,ave} = \frac{1}{2} P_{Static,on} + \frac{1}{2} P_{Static,off} = \frac{1}{2}\left(I_{PD,off} + I_{PU,on}\right) V_{DD}$$

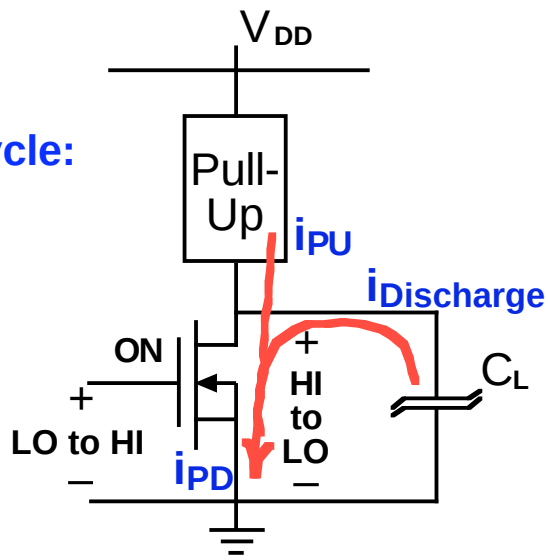
Inverter metrics: Power, cont.

Dynamic:

Charging cycle:



Discharging cycle:



$\frac{1}{2}C_L V_{DD}^2$ Dissipated, $\frac{1}{2}C_L V_{DD}^2$ Stored

$\frac{1}{2}C_L V_{DD}^2$ Dissipated

Energy dissipated per cycle: $C_L V_{DD}^2$

Cycles per second: f

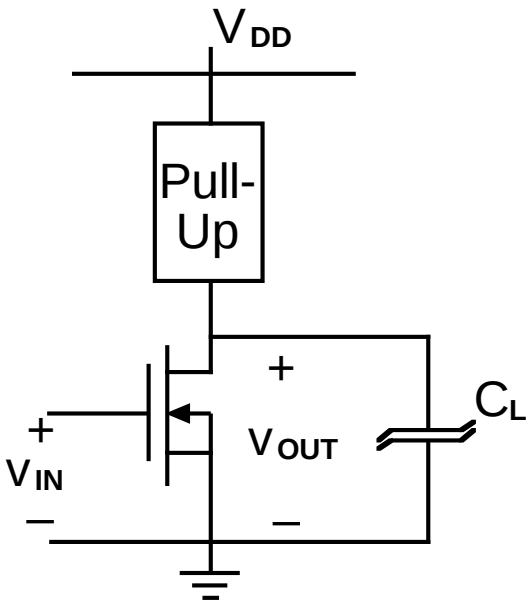
$$P_{Dynamic,ave} = f\, C_L V_{DD}^2$$

Total:

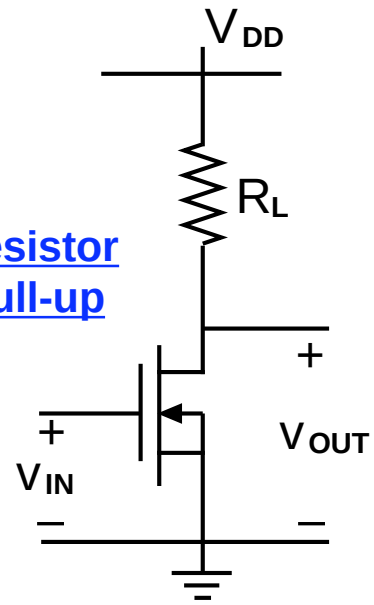
$$P_{Total} = \frac{1}{2}\left(I_{PD,off} + I_{PU,on}\right)V_{DD} + f\, C_L V_{DD}^2$$

MOS inverters:

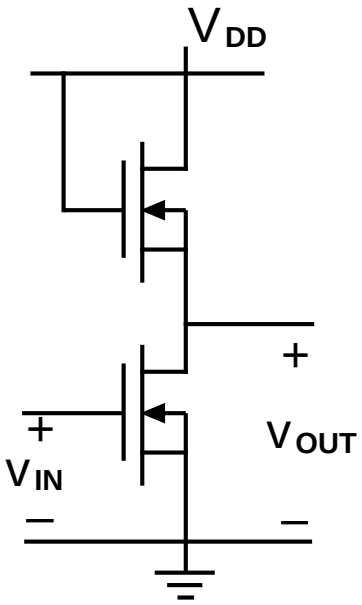
5 pull-up choices

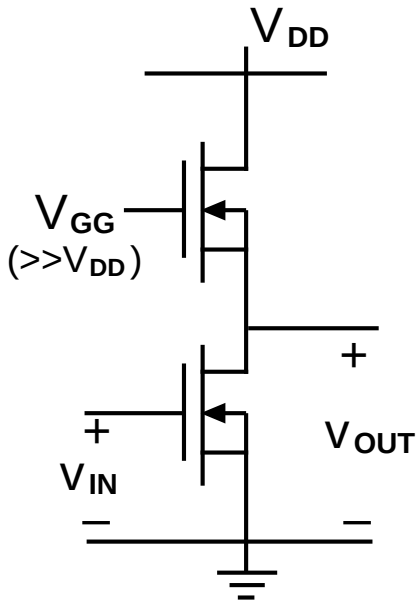


Generic inverter



Resistor pull-up

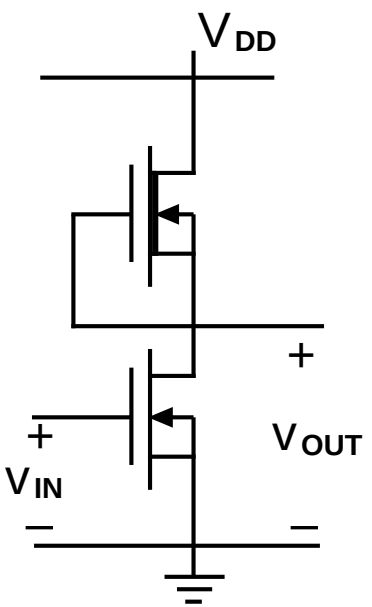




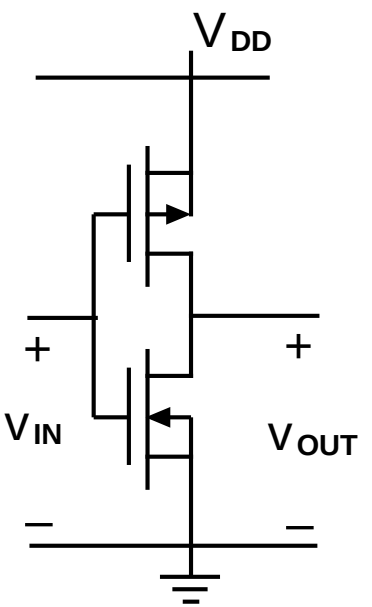
n-channel, e-mode pull-up*

V_{DD} on gate

V_{GG} on gate



n-channel, d-mode pull-up (NMOS)



Active p-channel pull-up (CMOS)**

* Called PMOS when made with p-channel FETs. ** Notice that CMOS has a larger (~3x) input capacitance.

MOS inverters: Comparing the 5 pull-up choices

Ground rules:

To make the comparison meaningful, we set the following conditions:

1. We use the same pull-down device with each of the different pull-ups.

2. We use the same fan out, n, to identical inverters to have a valid comparison of the amount of charge that must managed to charge and discharge, and of the dynamic power dissipation. We also assume the load capacitance, C_L, is linear and n times a single inverter input capacitance.

3. We use the same V_{HI} and $I_{PU,on}$ so the static power dissipation is the same.

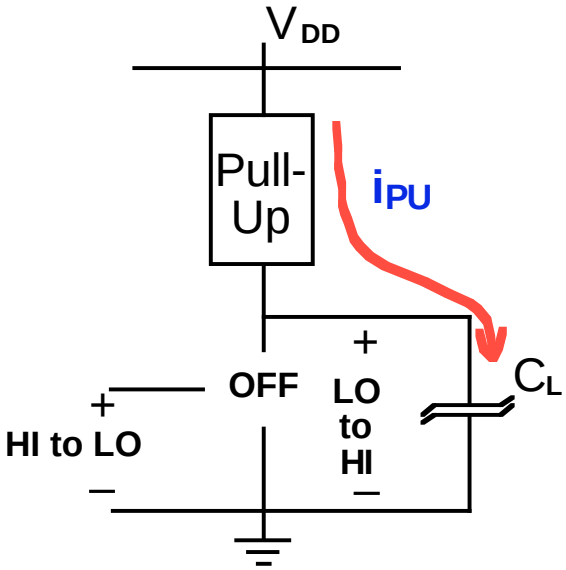
In this way we can see which pull-up gives us the highest speed, all else being equal.

Switching transients

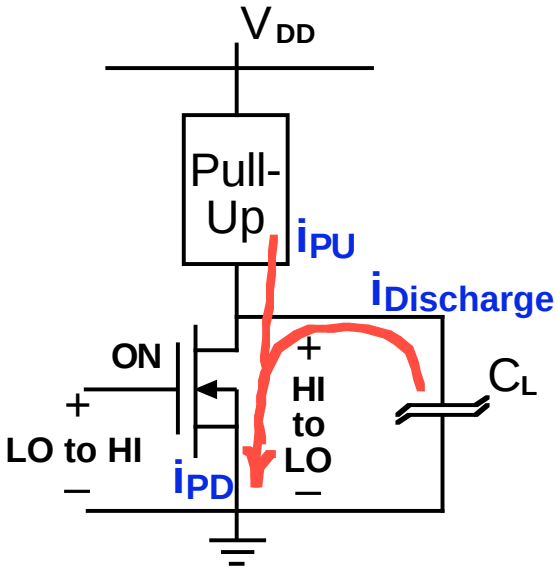
General approach

The load, C_L, is a non-linear charge store, but for MOSFETs it is fairly linear and it is useful to think linear:

$$\frac{dv_{OUT}}{dt} = i_{C_L}(v_{OUT}) / C_L$$



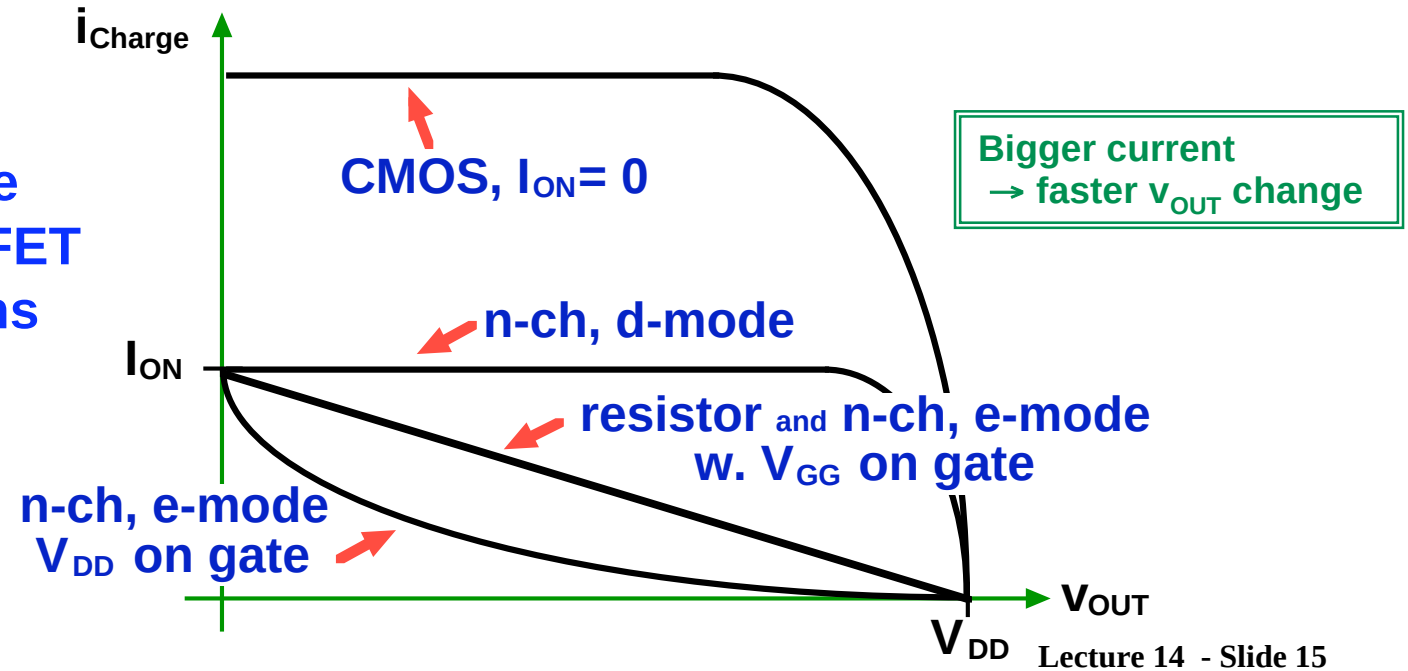
Charging cycle:
$i_{Charge} = i_{PU}$



Discharging cycle:
$i_{Discharge} = i_{PD} - i_{PU}$

Charging C_L:

The charging current for the various MOSFET pull-up options

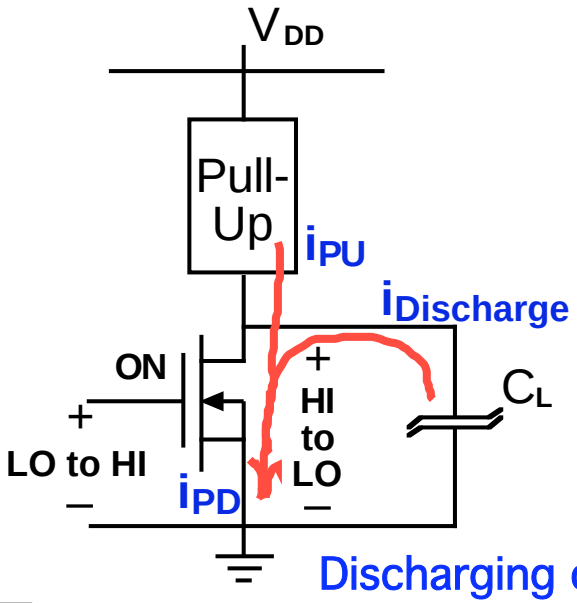


Switching transients, cont.

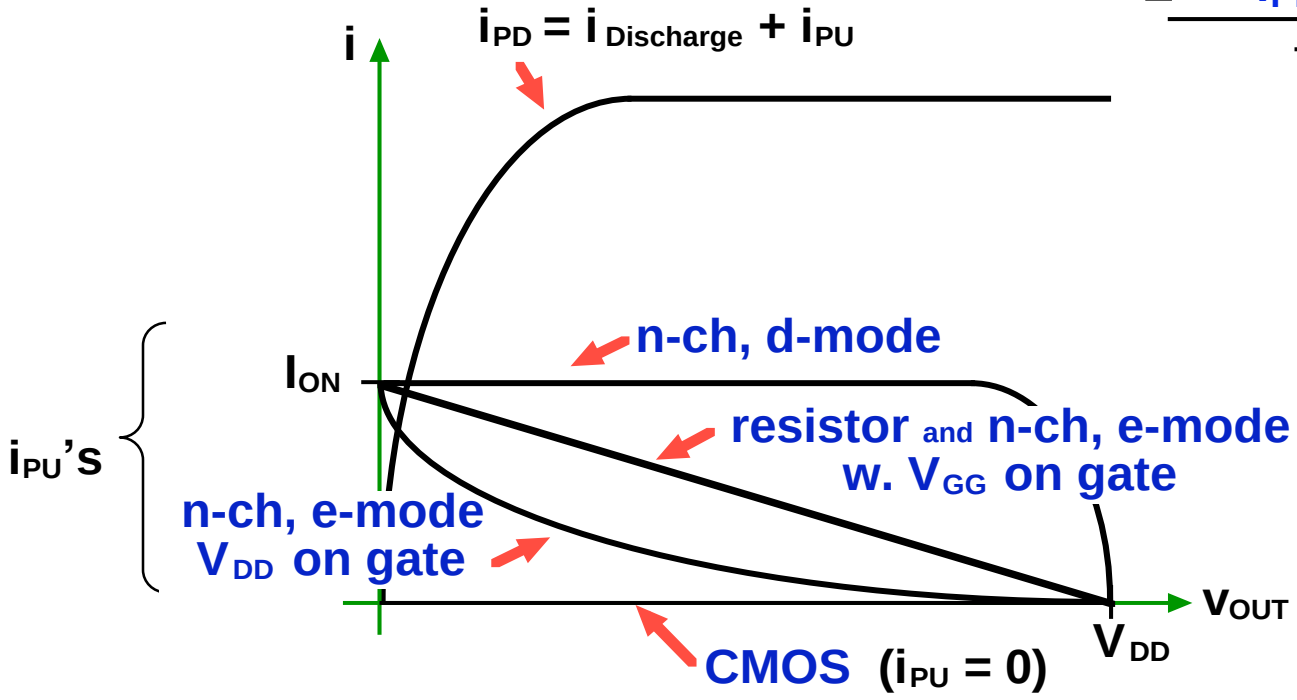
Discharging C_L:

This depends on the pull-up device, as well as the pull-down

The discharging current for the various pull-up options



Discharging cycle:
$i_{Discharge} = i_{PD} - i_{PU}$



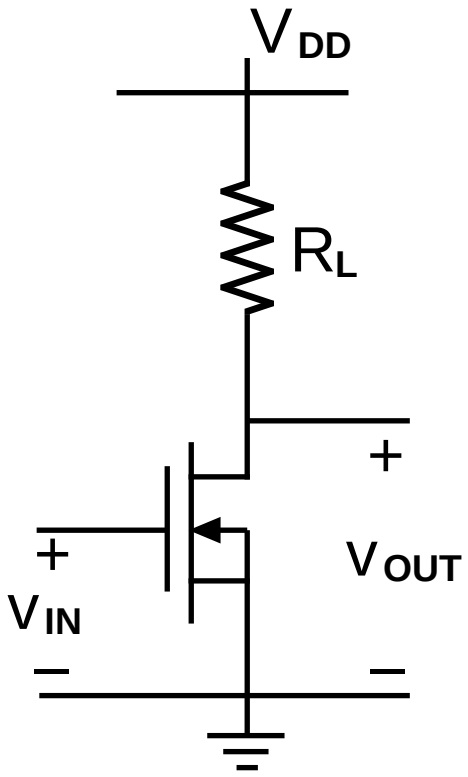
✓ **The discharge current ($i_{Discharge}$) is the difference between the upper curve (i_{PD}) and the appropriate lower curve (i_{PU}).**

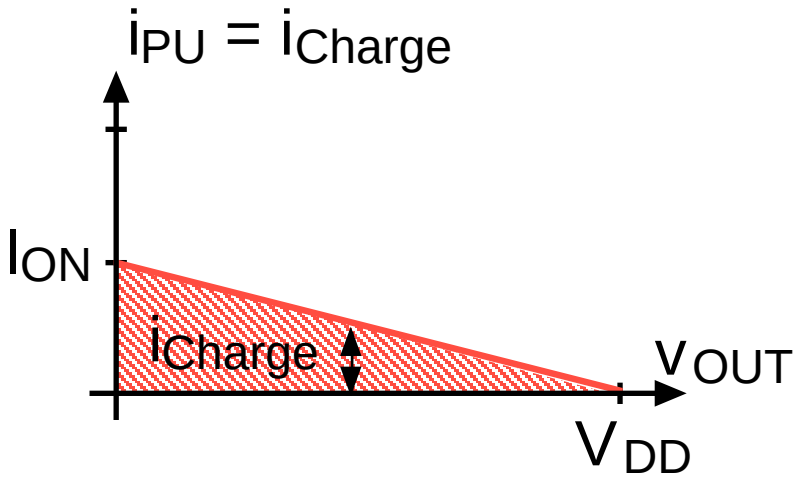
Which pull-up is best? To see we next look at each in turn and then compare them.

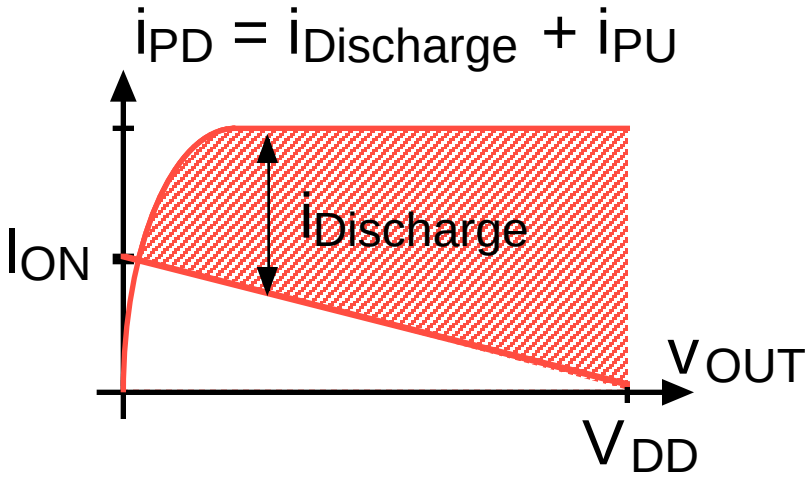
Switching transients, cont.

Charging and discharging:

Linear resistor pull-up







Simple

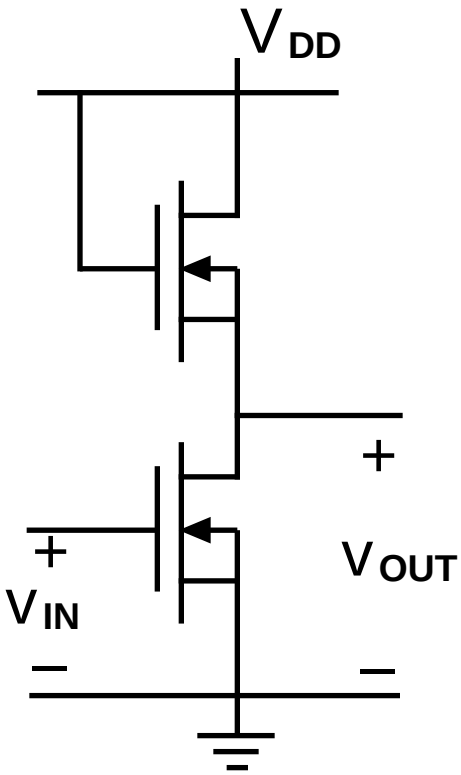
Least costly with discrete components but integrated resistors consume lots of space.

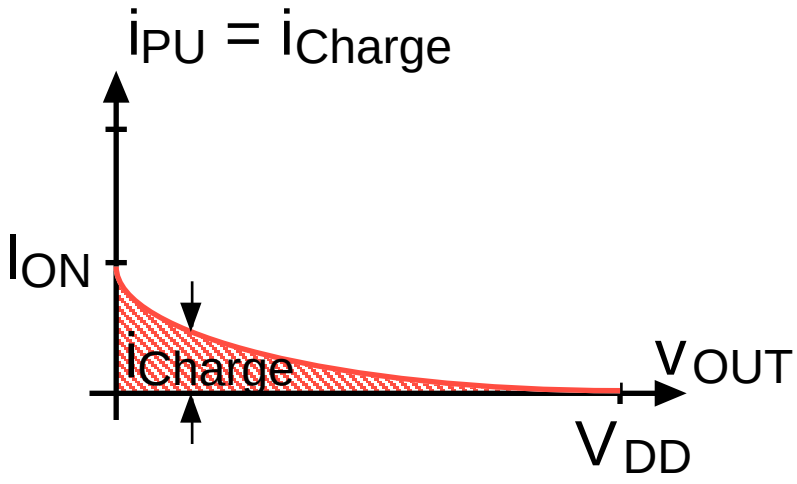
$\tau_{Charge} >> \tau_{Discharge}$

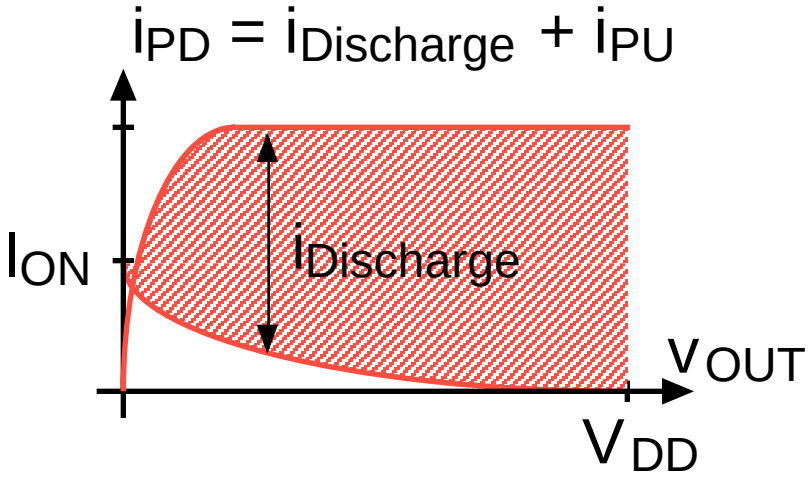
Switching transients, cont.

Charging and discharging:

Saturated E-mode pull-up







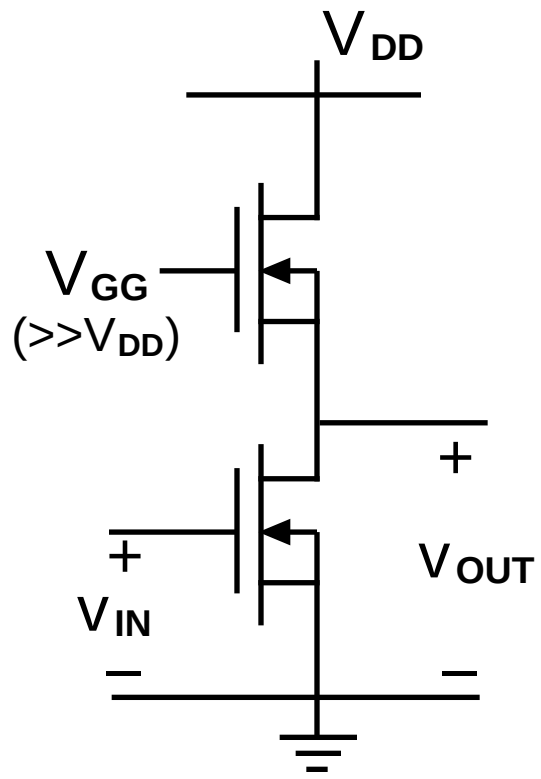
No added cost in adding more MOSFETs
Very compact
No added wiring
Slower than linear resistors

$\tau_{Charge} >>> \tau_{Discharge}$

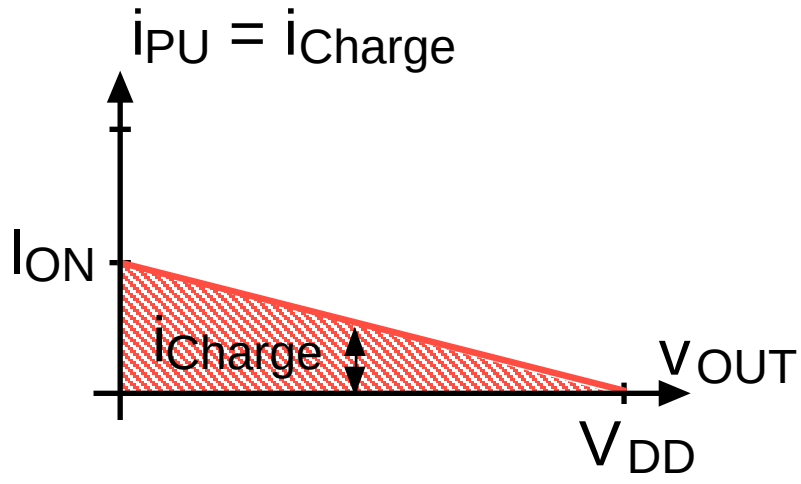
Switching transients, cont.

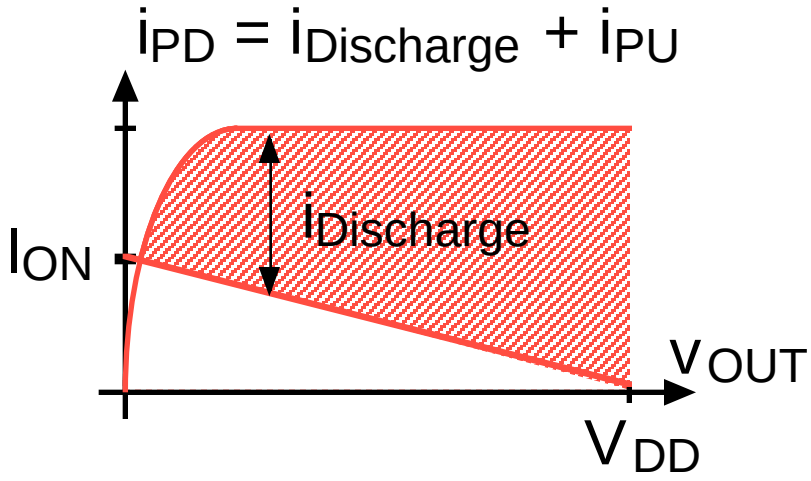
Charging and discharging:

Linear E-mode pull-up



Still compact
Need to wire VGG to each gate
Need second supply
Not faster than linear resistor



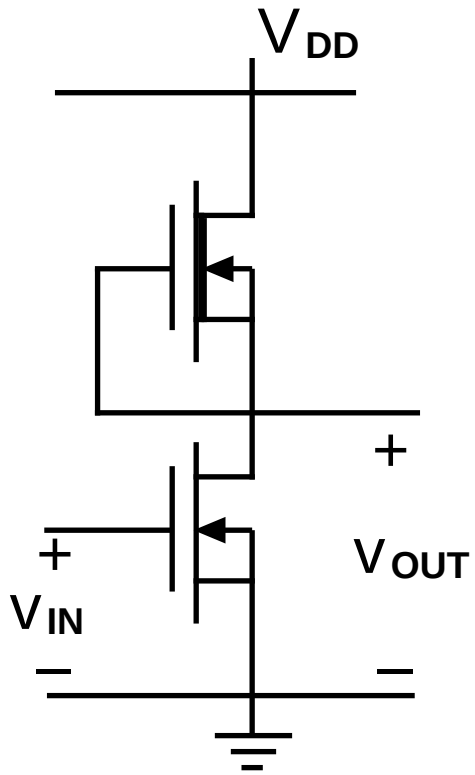


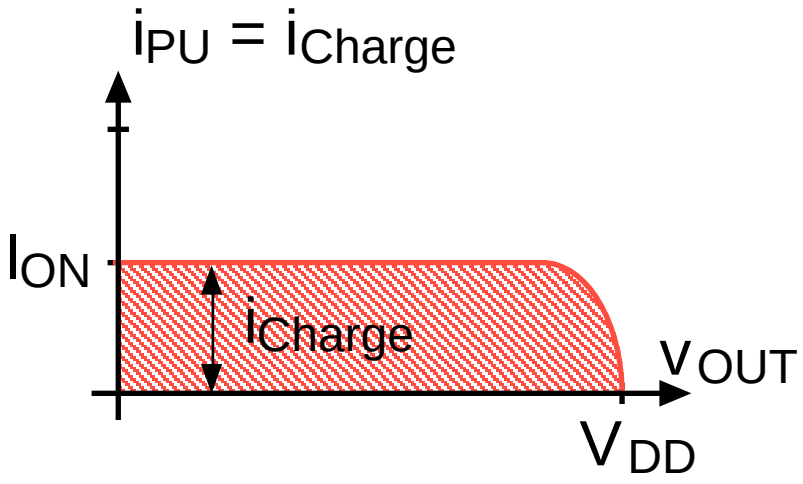
$\tau_{Charge} >> \tau_{Discharge}$

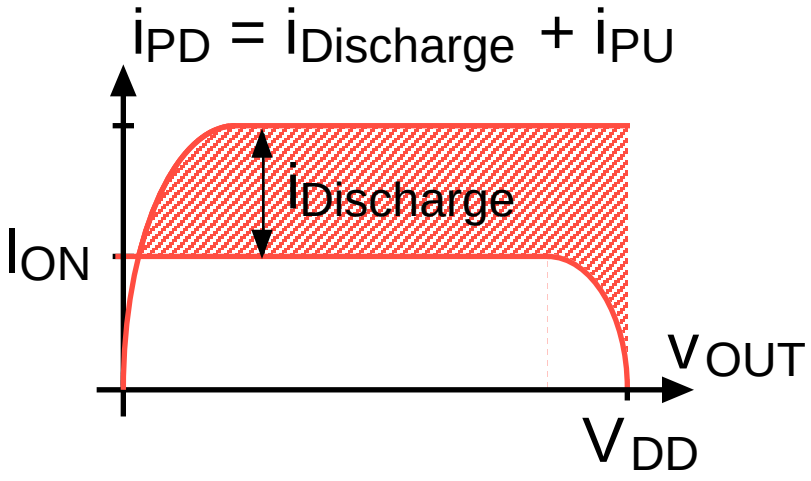
Switching transients, cont.

Charging and discharging:

D-mode pull-up ("NMOS")







Compact
Symmetrical charge/discharge
Fastest possible
Must make E- and D-mode on safe wafer

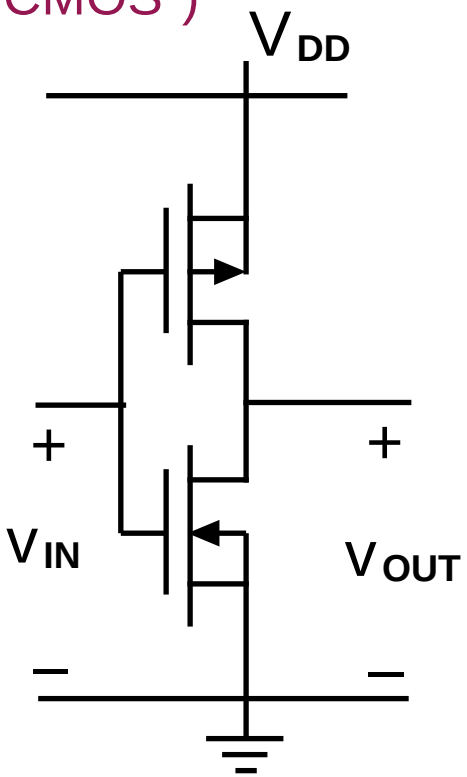
$\tau_{Charge} \approx \tau_{Discharge}$

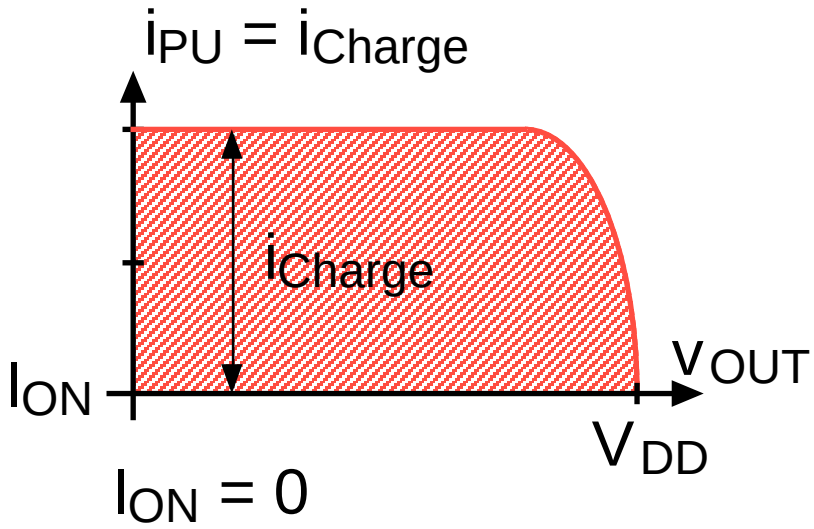
Switching transients, cont.

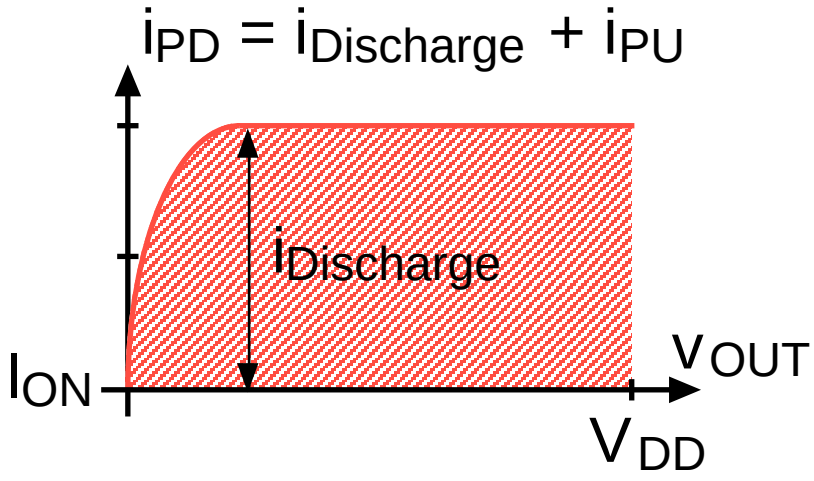
Charging and discharging:

Active complementary pull-up

("CMOS")







Symmetrical charge/discharge

Almost as fast, or even faster than, n-MOS*

MInimal static power dissipation ($I_{ON} \approx 0$)

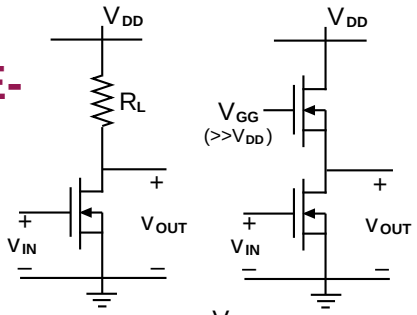
Must make n- and p-channel on same wafer

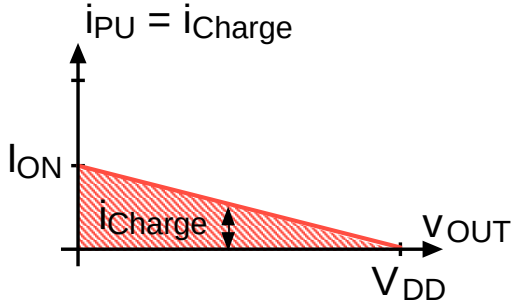
$\tau_{Charge} \approx \tau_{Discharge}$

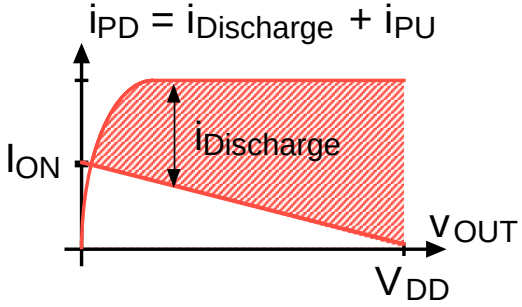
* The input capacitance is 3x larger, but the interconnect capacitance is the same, so it depends on which of the two is dominant.

Switching transients: summary of charge/discharge currents

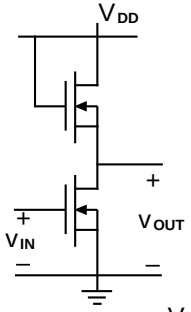
Resistor and E-mode pull-up (V_{GG} on gate)

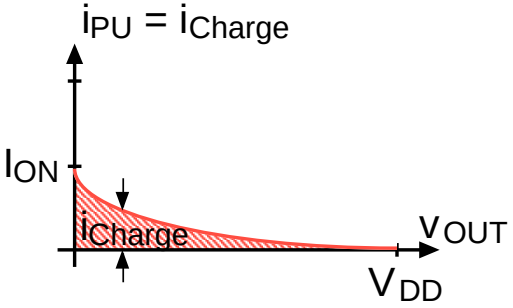


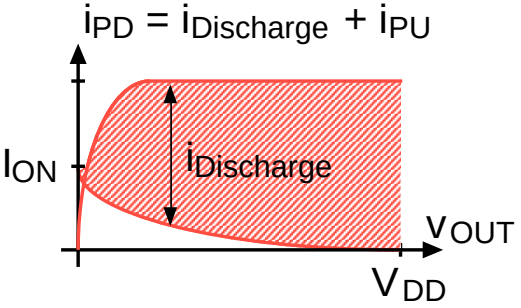




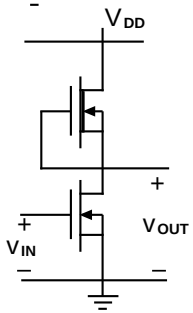
E-mode pull-up (V_{DD} on gate)

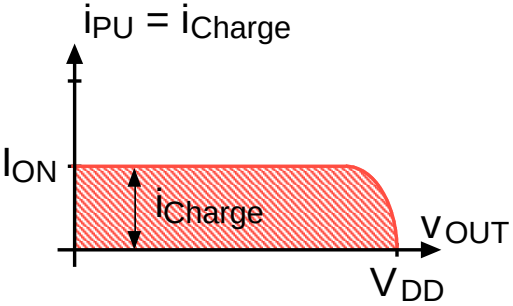


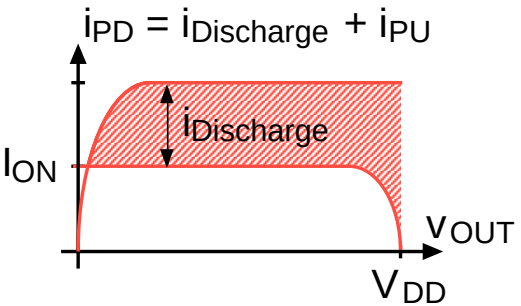




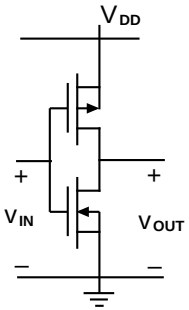
D-mode pull-up (called "NMOS")

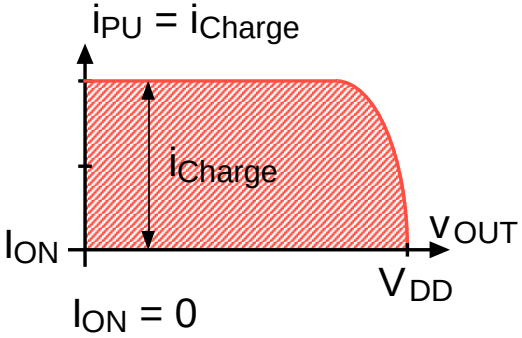


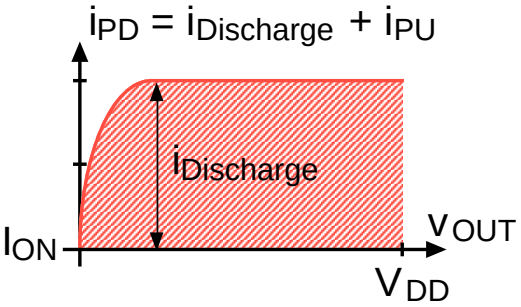




CMOS







- Comparisons made with same pull-down MOSFET, V_{HI}, and I_{ON}.

MOS Technology: An abbreviated history

p-MOS:

In the beginning (mid-60s) there were only metal-gate p-channel e-mode MOSFETs; n-channel MOSFETs came out d-mode. p-MOS logic relied on saturated and linear e-mode pull-ups.

n-MOS:

With the development of <100> substrates, e-beam deposition, self-aligned poly-Si gates, and ion implantation, initially to improve p-MOS, it became possible to also reliably fabricate e-mode n-channel FETs. NMOS, with d-mode pull-ups, then took off (ca 1970).

CMOS:

It was clear for many years that CMOS inverters were superior, but fabricating them reliably in high density and at low cost was a big challenge. Eventually manufacturers learned how to make n- and p-channel MOSFETS together in close proximity and economically (ca 1980); CMOS then soon became the dominant IC technology because of its superior low power and high speed.

For the past decade the industry has been fixated on systematically making FETs smaller, circuits more dense, and wafers larger.*

* And with good reason; more next week in Lecture 17.

Lecture 14 - Digital Circuits: Inverter Basics - Summary

- **Digital building blocks - inverters**
  - **A generic inverter:** Switch = pull-down device, Load = pull-up device
  - **MOS inverter options - Pull-down:** n-channel, e-mode **(faster than p-channel)**
    - **Pull-up:** 1. resistor; 2. n-channel, e-mode w. and w.o. gate bias; 3. n-channel, d-mode (NMOS); 4. p-channel, e-mode (CMOS)
- **Digital inverter performance metrics**
  - **Transfer characteristic**
    - **Logic levels:** V_{HI}, V_{LO}
    - **Noise margins:** NM_{HI} (high), and NM_{LO} (low)
    - **Design variables:** choice of pull-up device
      pull-up and pull-down thresholds
      device sizes (absolute and relative)
  - **Power dissipation:** stand-by power and switching dissipation
  - **Switching speed:** capacitive load
    charge and discharge currents critical
  - **Fan-out, fan-in:** minimal issue in MOS; more so with BJT logic
  - **Manufacturability:** small, fast, low-power, reliable, and cheap
- **Comparing the MOS options**
  - **And the winner is….CMOS**

6.012 Microelectronic Devices and Circuits

Fall 2009