3.155J/6.152J Lecture 22: Take Home Exam Discussion

Prof. Martin A. Schmidt Massachusetts Institute of Technology 12/5/2005



- Review of Schedule
- The Knowles Microphone



- Week of 12/5
 - Monday Take Home Discussion
 - Wednesday Prof. Joel Voldman Biological and Medical Applications of Micro/Nano Fab
 - Fluids Lab Due
 - Course Evaluation
- Week of 12/12
 - Monday Prof. Leslie Kolodziejski Photonic Devices and Compound Semiconductors
 - Wednesday Analog Devices Tour
 - Take Home Due



Take Home Design Challenge

- Design a process for fabrication of a microphone integrated with a depletion mode nMOSFET
- Utilize the Knowles microphone as our model device
 - U.S. Patent 6,847,090
 - 'Silicon Capacitive Microphone' Loeppert



Microphone Cross-Section

Figure removed for copyright reasons.



Microphone Cross-Section

Figure removed for copyright reasons.





Loeppert "Silicon Capacitive Microphone." U.S. Patent 6,847,090.

How are the electrical connections made?



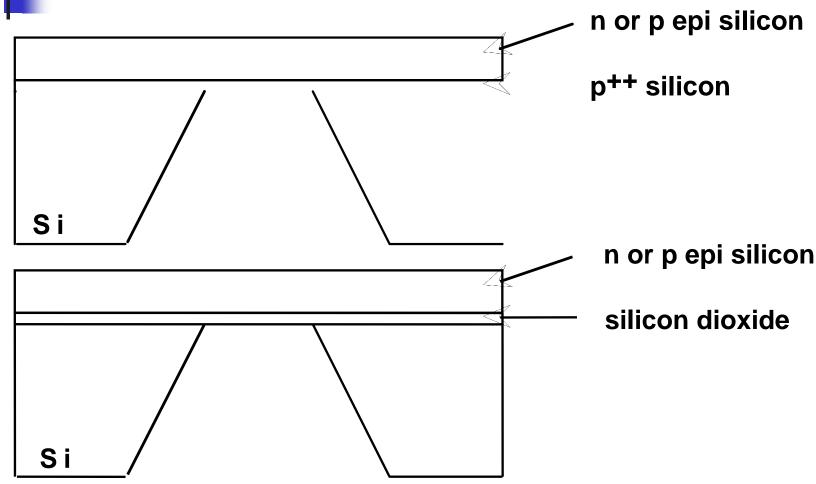
- Membrane (1)
 - Stress-compensated boron-doped etch stop
 - Lightly doped silicon with buried etch stop
 - Boron-doped silicon or oxide
- Backplane (2)
 - Boron-doped silicon



Figure found in H. Seidel, L. Csepregi, A.Hueberger, and H. Baungärtel. *The Journal of the Electrochemical Society* 137 (1990): 3612-3626.



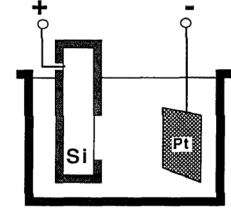
Buried Etch Stops

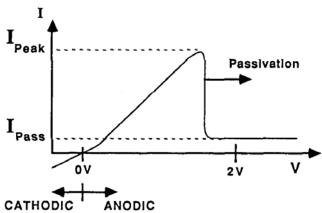


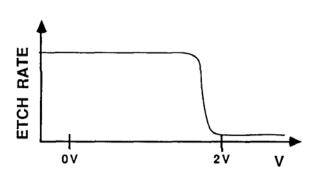
Masking material: silicon dioxide or silicon nitride

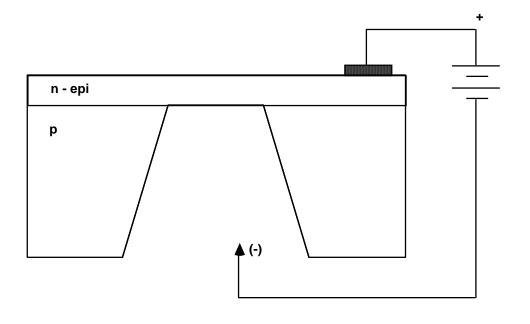


Electrochemical Etch-stop









Fall 20



- Pattern insulating layer (oxide)
- Etch trenches



- Silicon Fusion Bonding
 - Clean (RCA) both wafers
 - Contact
 - Reduced atmosphere ambient
 - Anneal 1000C, 1hour



Loeppert "Silicon Capacitive Microphone." U.S. Patent 6,847,090.

Substrate Etch

- Masking material
- Boron etch stop (N > 10^{20} cm⁻³)
- Alternatives
 - SOI, Electrochemical



Loeppert "Silicon Capacitive Microphone." U.S. Patent 6,847,090.

Trench Etch



Integration with nMOS

- Isolation
 - Can utilize oxide isolation
- Move cavity etch to end of process
 - Requires a means to protect the wafer frontside
- Interconnect
 - Need to connect FET to capacitor plate, and provide metal covered connections to other plates of capacitor
- Process 'ease'
 - Some steps hard (e.g. handling a wafer with holes)



- Complete Take Home Problem Statement will be handed out / posted on Wednesday
- Solution due on Wednesday