3.155J/6.152J Lecture 5: IC Lab Testing

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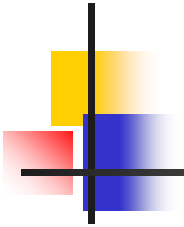
9/26/2005

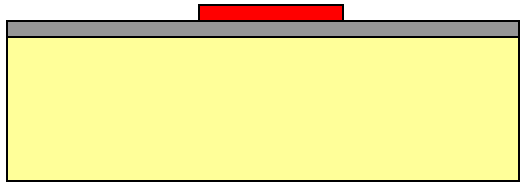


Outline

- Review of Process
- Structures to be Tested
- Sheet Resistance
- MOS Capacitor

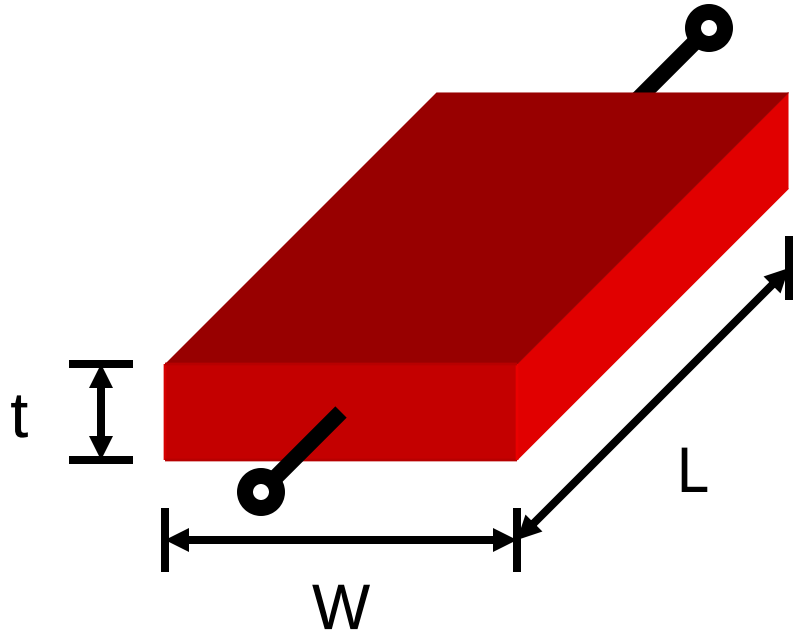
Our Process

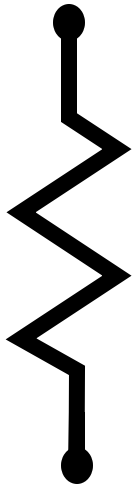
- Polysilicon Gate (n-type) MOS Capacitor
  - n-type substrate
  - 250nm n-type polysilicon gate
  - 50nm gate oxide



- Various size capacitors
- Polysilicon sheet resistivity monitor

Resistance





$$R = \underline{\rho}\ L/A = \underline{(\rho/t)}\ \underline{(L/W)}$$

Resistivity
Ω-cm

Process

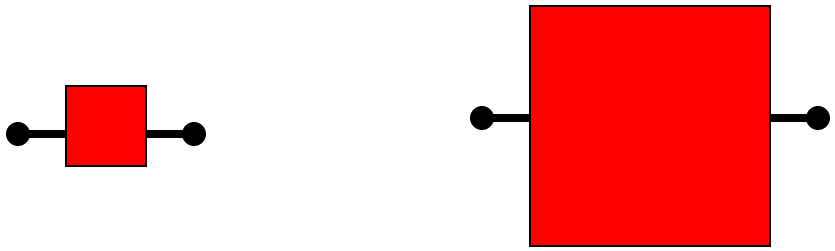
Mask

Concept of Sheet Resistivity

$$R = \rho\, L/A = (\rho/t)\ (L/W)$$

Sheet Resistivity (R_S)
Ω/sq

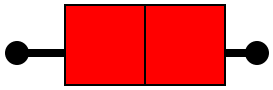
\# of Squares



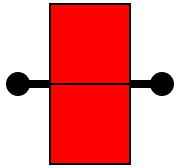
$$L = W$$

$$R = R_S$$

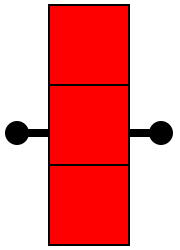
Number of Squares



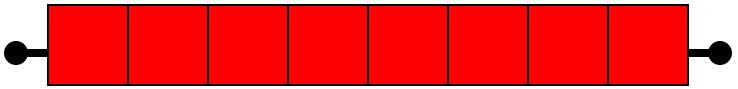
$R = 2R_S$



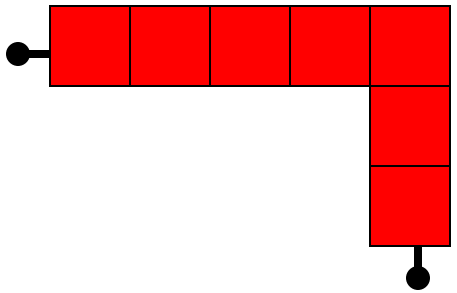
$R = R_S/2$



$R = R_S/3$

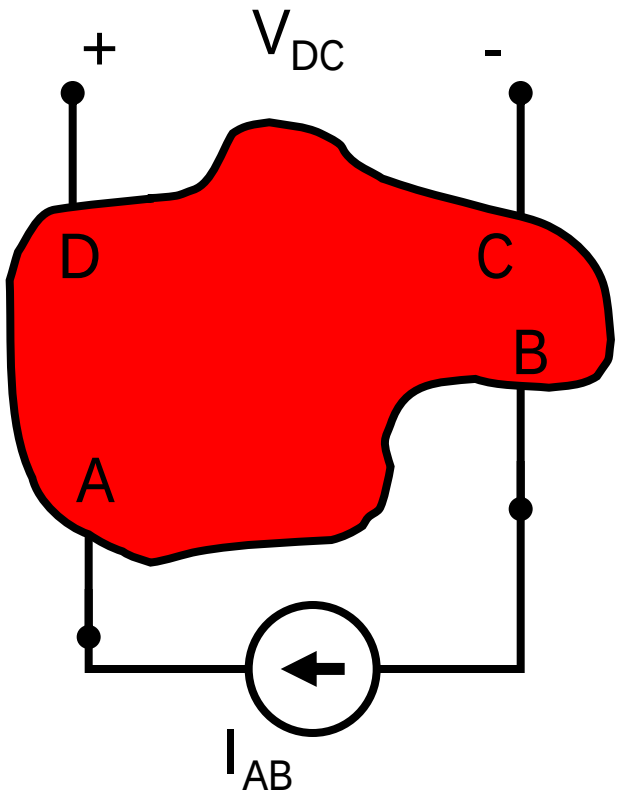


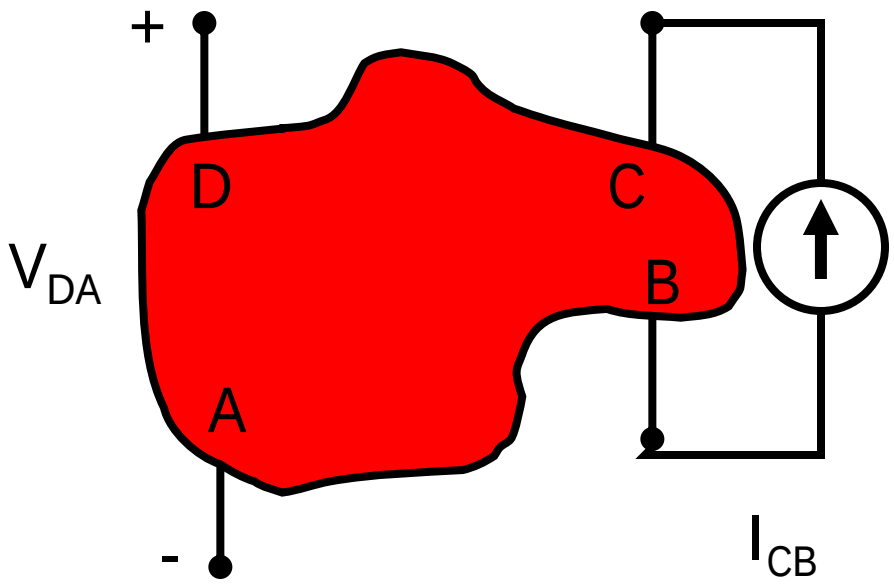
$R = 8R_S$



$R = 6.5R_S$

Measurement of Sheet Resistance





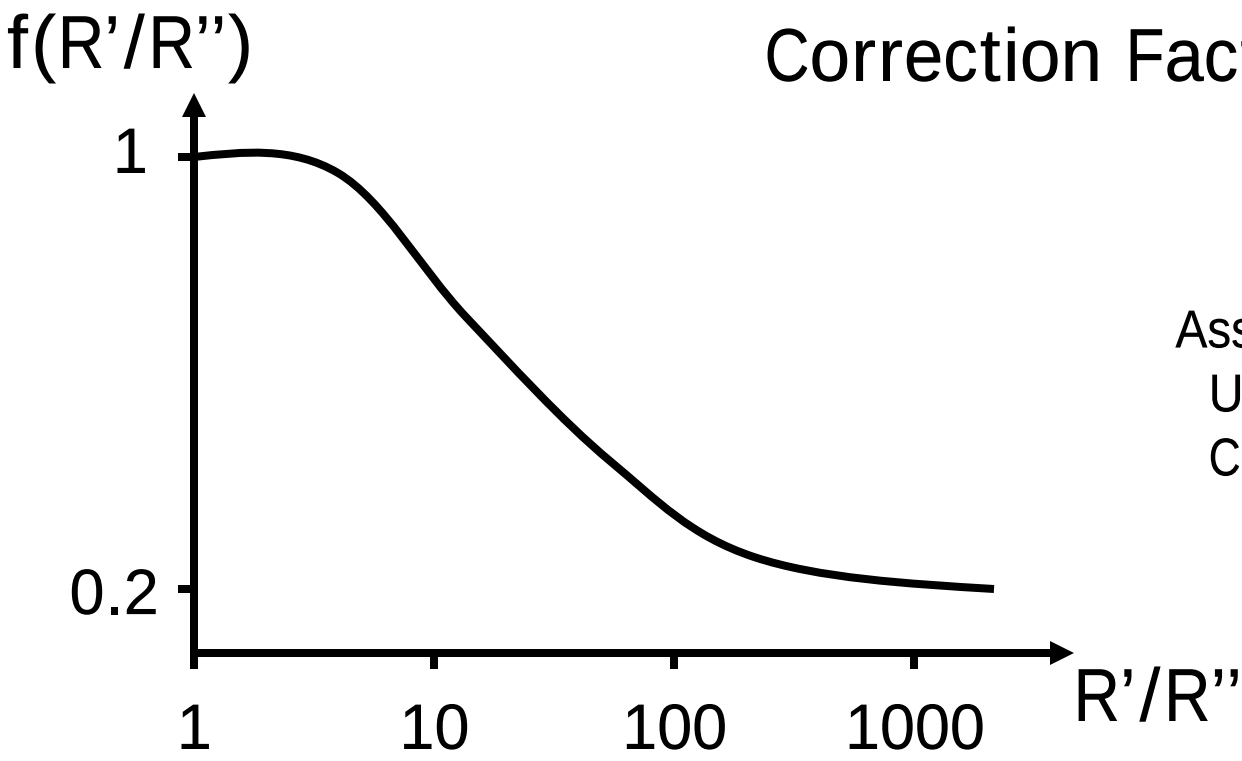
$$R' = V_{DC} / I_{AB}$$

$$R'' = V_{DA} / I_{CB}$$

Van der Pauw

$$R_S = (\pi/\ln 2)\ \tfrac{1}{2}\ (R'+R'')\ f(R'/R'')$$

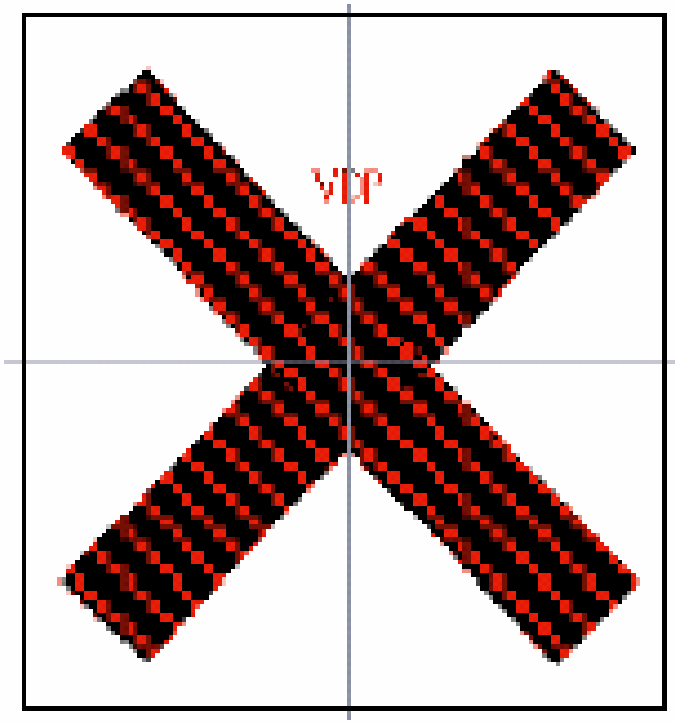
Correction Factor



Assumptions:
- Uniform thickness
- Continuous (no holes)

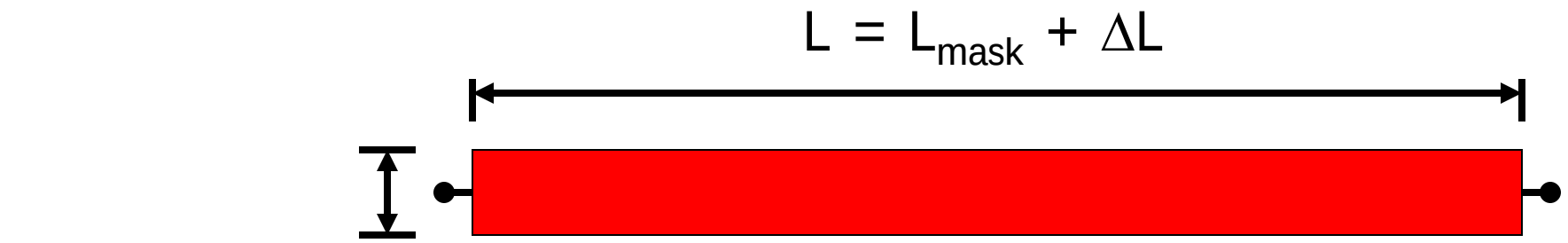
Van der Pauw

- Implement a symmetric structure
  - R' = R''
  - f(R'/R'') = 1
- $R_S = 4.53\ R_{ave}$
- $R_{ave} = \frac{1}{2}\ (R'+R'')$



Van der Pauw test structure. Arms should align to pins 7, 5, 21, and 15.

N Square Resistor

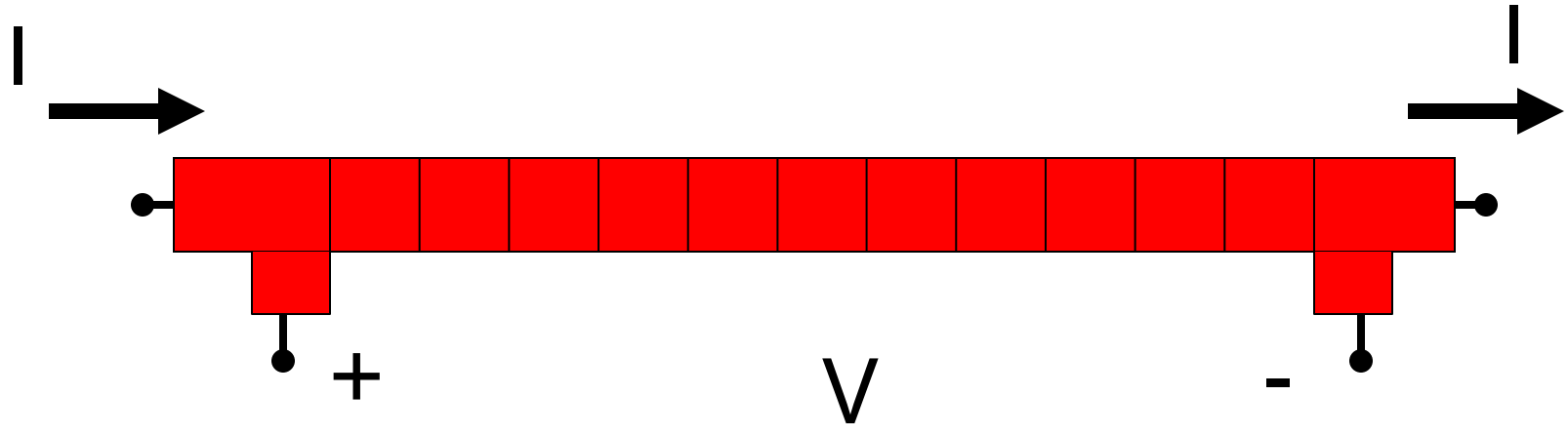


$N = L_{mask}/W_{mask} >> 1$

$$R = R_S\,(L/W) = R_S\,[L_{mask}/(W_{mask} + \Delta W)]$$

Used to determine the process 'bias' (ΔW)

4-Point Probe



Eliminates the effect of contact resistance

Analysis of Resistivity

- Semiconductor Resistivity(ρ)/Conductivity(σ)
  - $1/\rho = \sigma = q(\mu_n n + \mu_p p)$
- N-type
  - $n >> p$
  - $\sigma = q\mu_n n$
- Single Crystal Silicon
  - n=N (doping density)
  - $\mu_{Si} = f(N)$
- Polysilicon
  - $\mu_{poly} << \mu_{Si}$

Single Crystal Silicon

Figure removed for copyright reasons.

Please see: Figure 3-5 in Pierret, Robert, and Gerold Neudeck. *Modular Series on Solid State Devices*. Reading, MA: Addison-Wesley, 1982. ISBN: 0201052873.

R. Pierret

Single Crystal Silicon

Figure removed for copyright reasons.

Please see: Plummer, J., M. Deal, and P. Griffin. *Silicon VLSI Technology: Fundamentals, Practice, and Modeling.* Upper Saddle River, NJ: Prentice Hall, 2000. ISBN: 0130850373.

Plummer

Poly Resistivity vs Dep. Temp.

Figure removed for copyright reasons.

Please see: Kamins, T. *Polysilicon for Integrated Circuit Application*. Norwell, MA: Kluwer Academic Publishers, 1988.

T. Kamins
Kluwer

Polysilicon Resistivity vs Dopant

Use for lab report

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Please see: Kamins, T. *Polysilicon for Integrated Circuit Application*. Norwell, MA: Kluwer Academic Publishers, 1988.

T. Kamins
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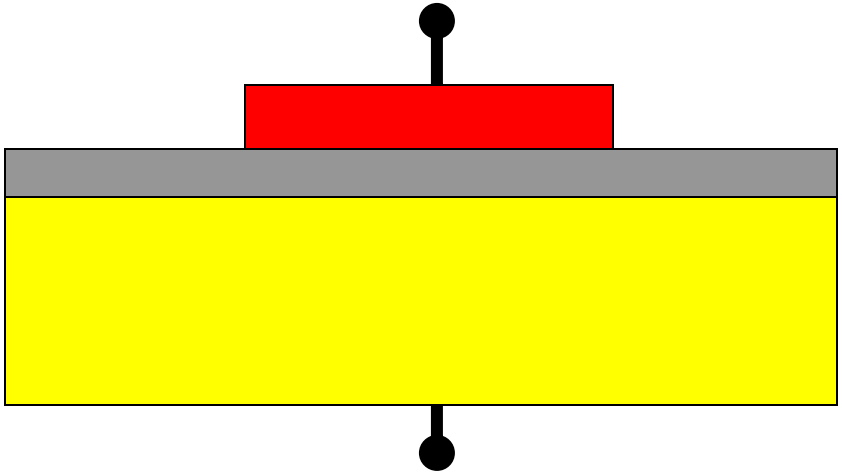
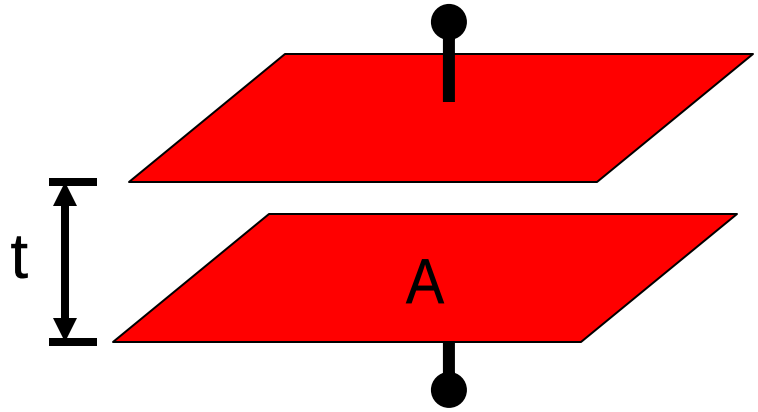
MOS Capacitor



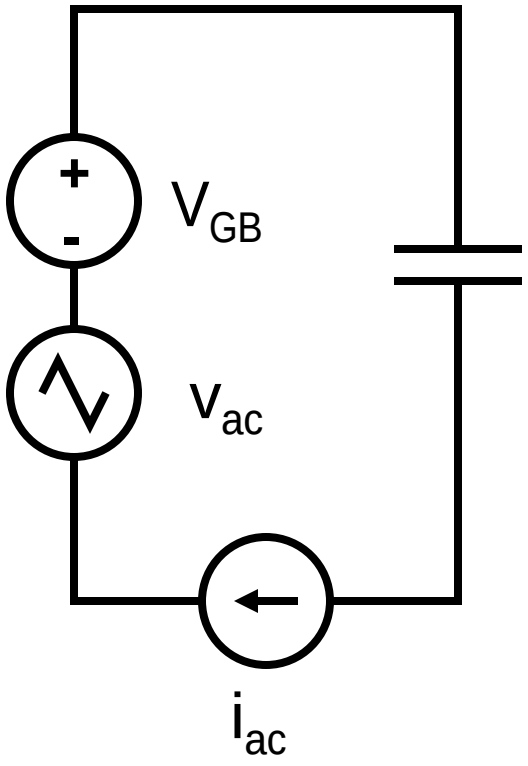


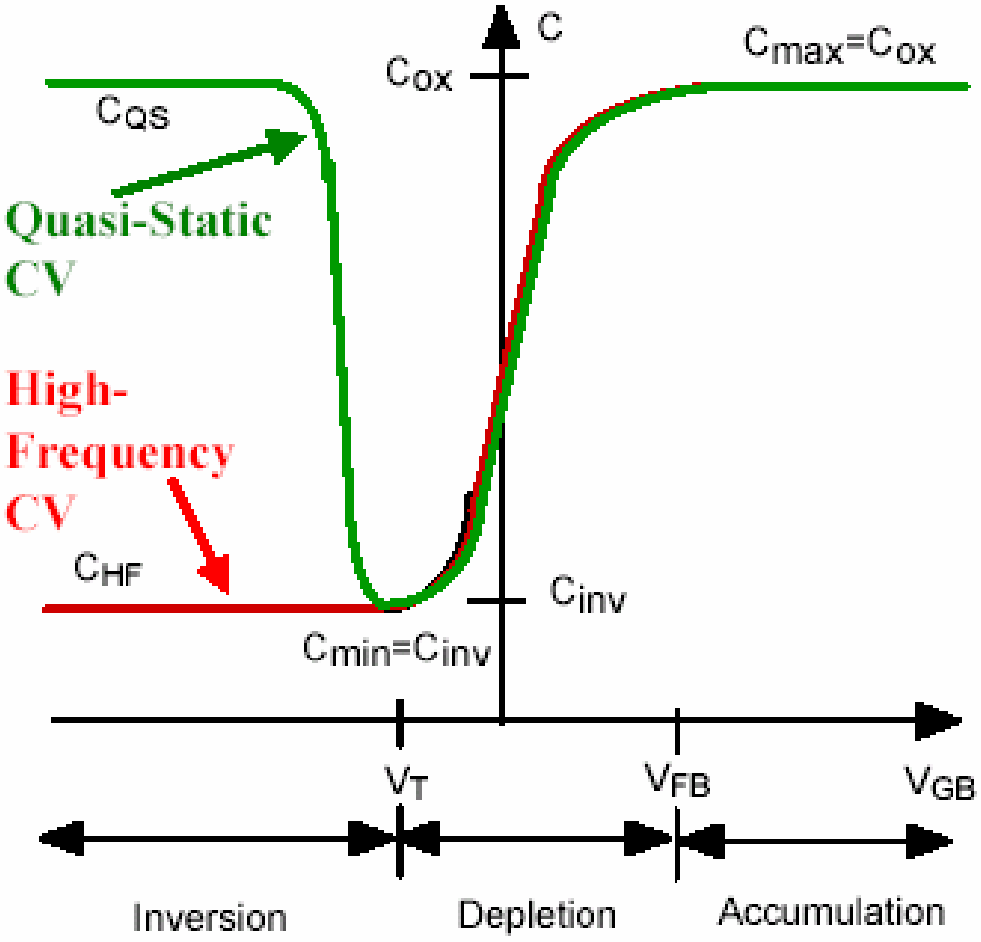
$$C = \varepsilon A/t = \varepsilon_r \varepsilon_o A/t$$

$$C^* = C / A$$

$$\varepsilon_r\ (SiO_2) = 3.9 \qquad \varepsilon_o = 8.85 \times 10^{-14}\ F/cm$$

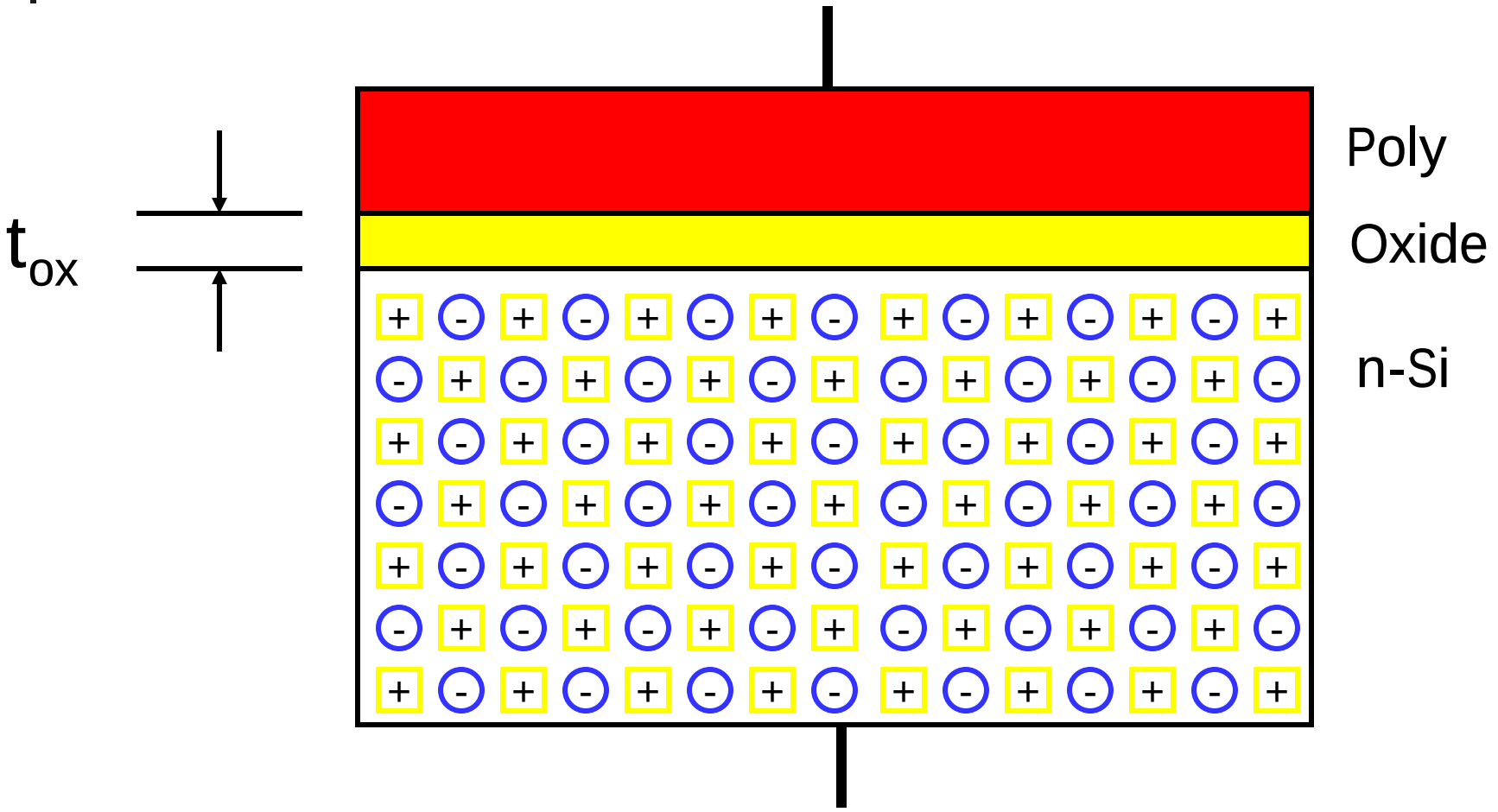
MOS Capacitance Measurement





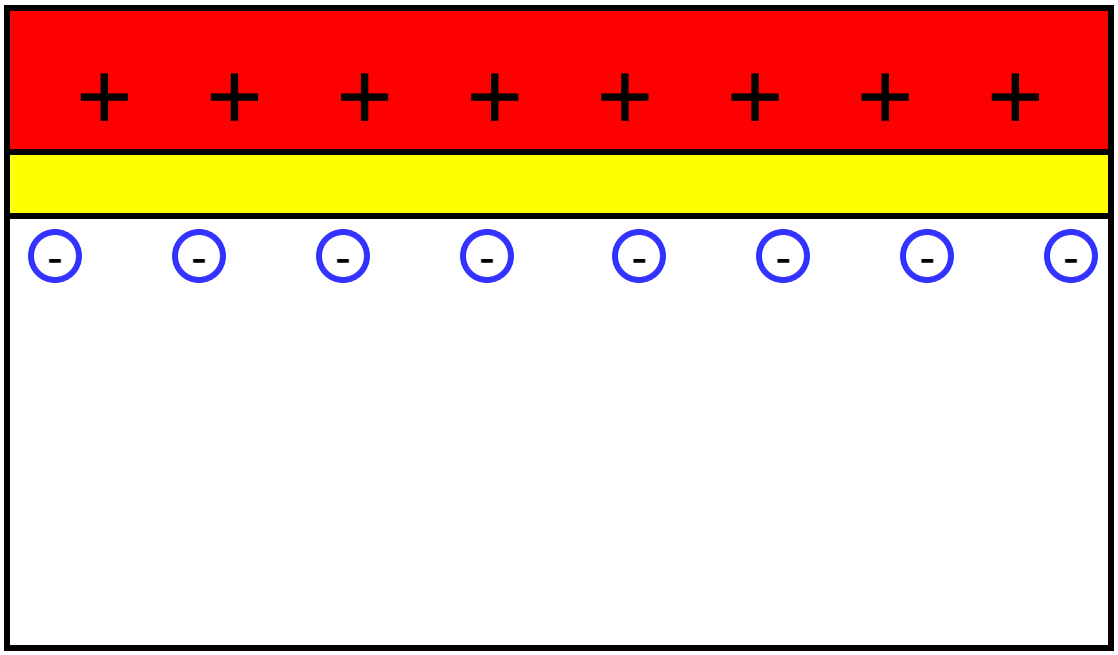
Ref: A. Akinwande

MOS Capacitor



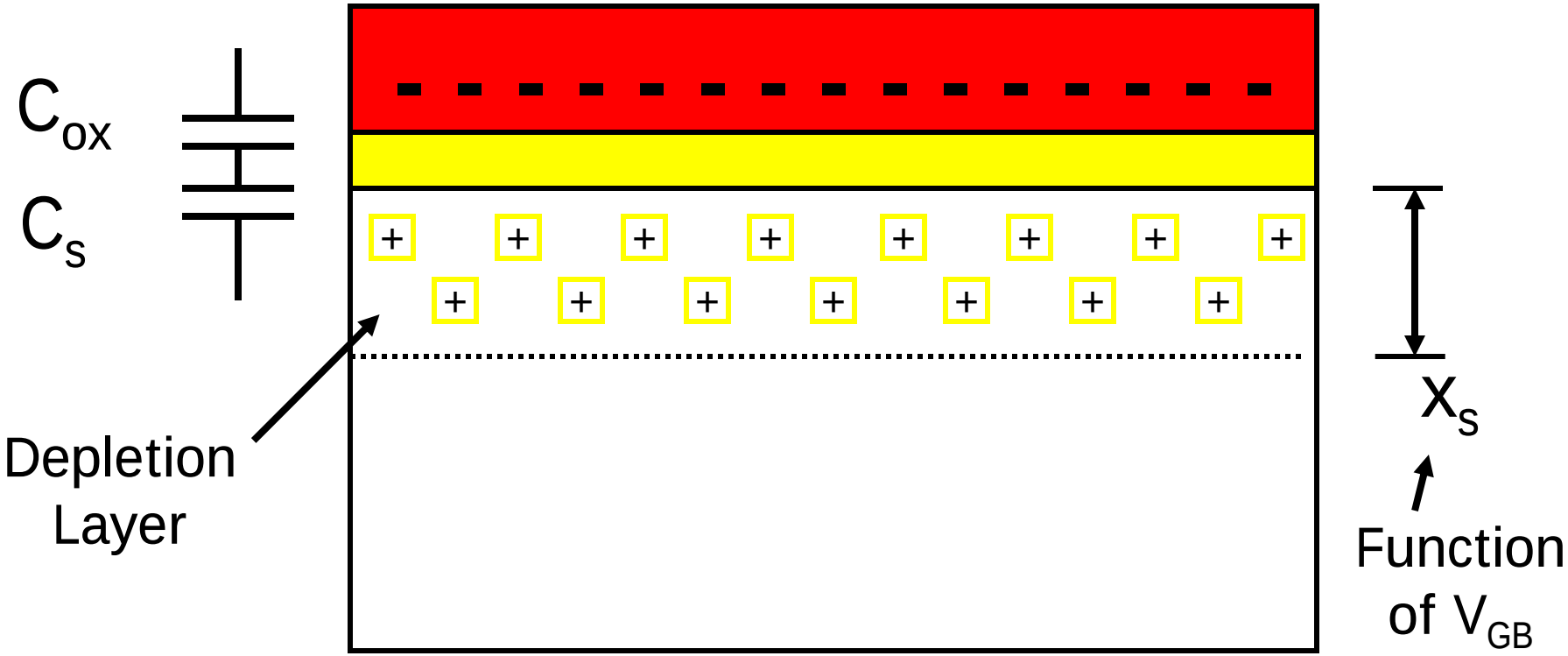
$$C^* = C / A$$

MOS Capacitor in Accumulation



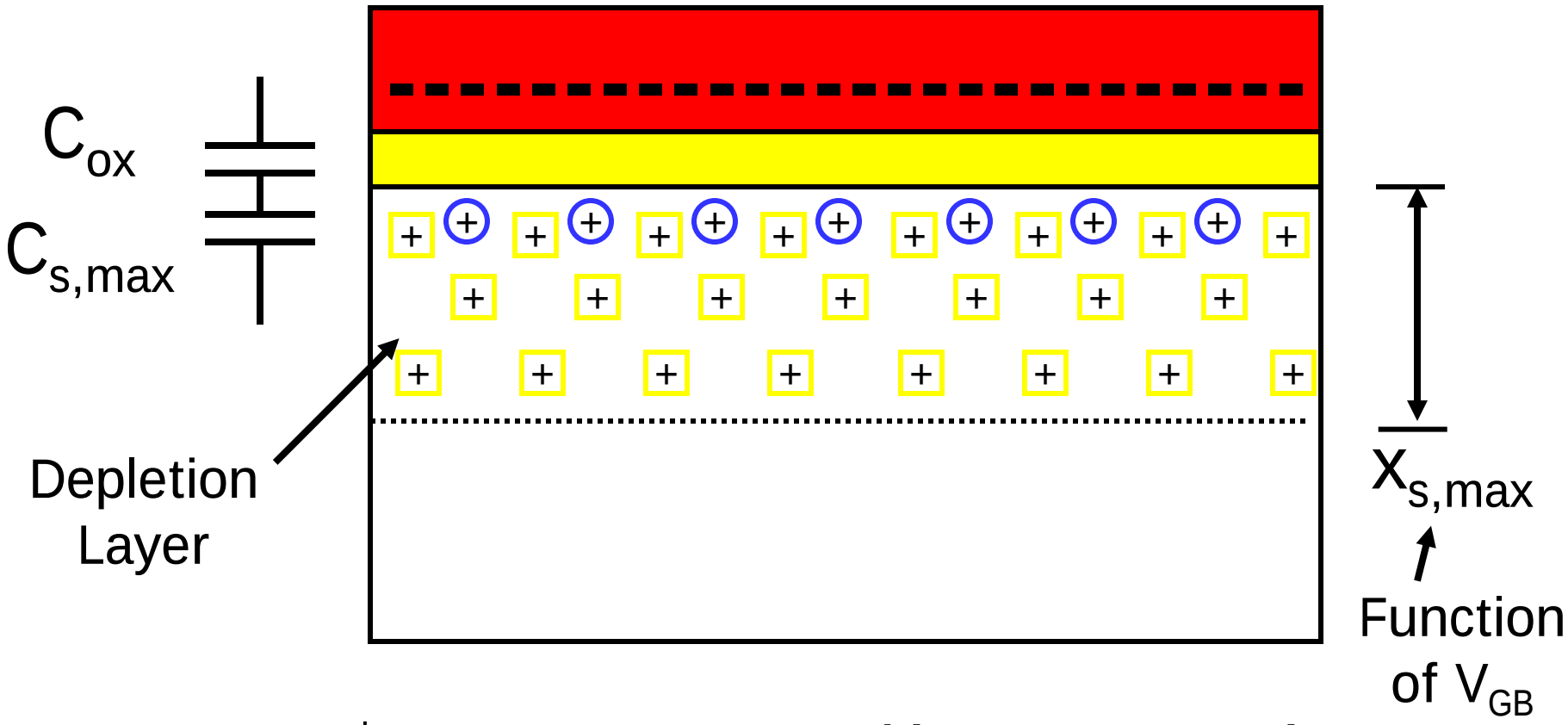
$$C^* = C_{ox} = \varepsilon_{ox} / t_{ox}$$

MOS Capacitor in Depletion



$$C^* = C_{ox}\, C_s / (C_{ox} + C_s) \qquad C_s = \varepsilon_{Si} / x_s$$

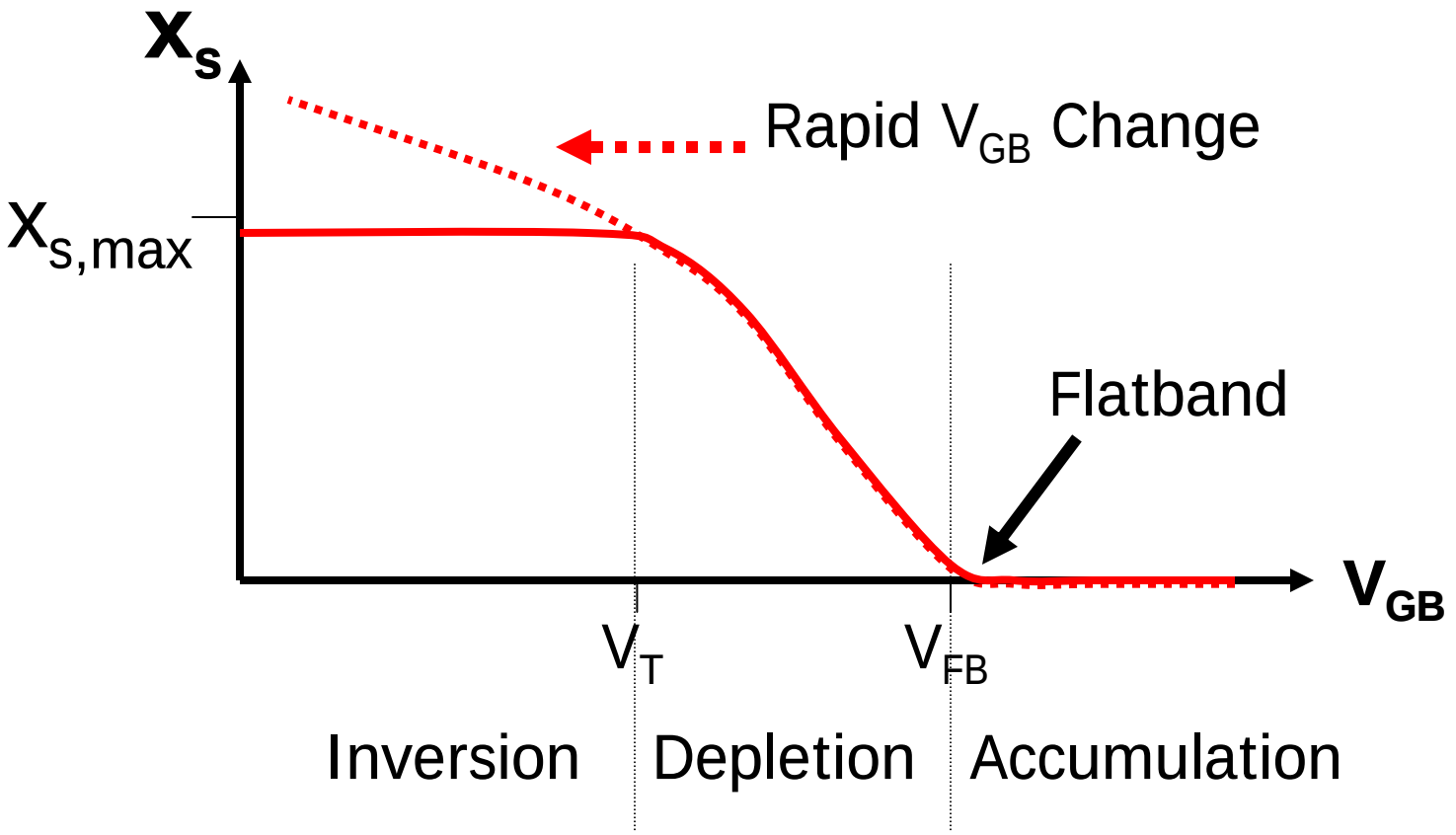
MOS Capacitor in Inversion



$$C^*_{min} = C_{ox}\, C_{s,max} / (C_{ox} + C_{s,max})$$

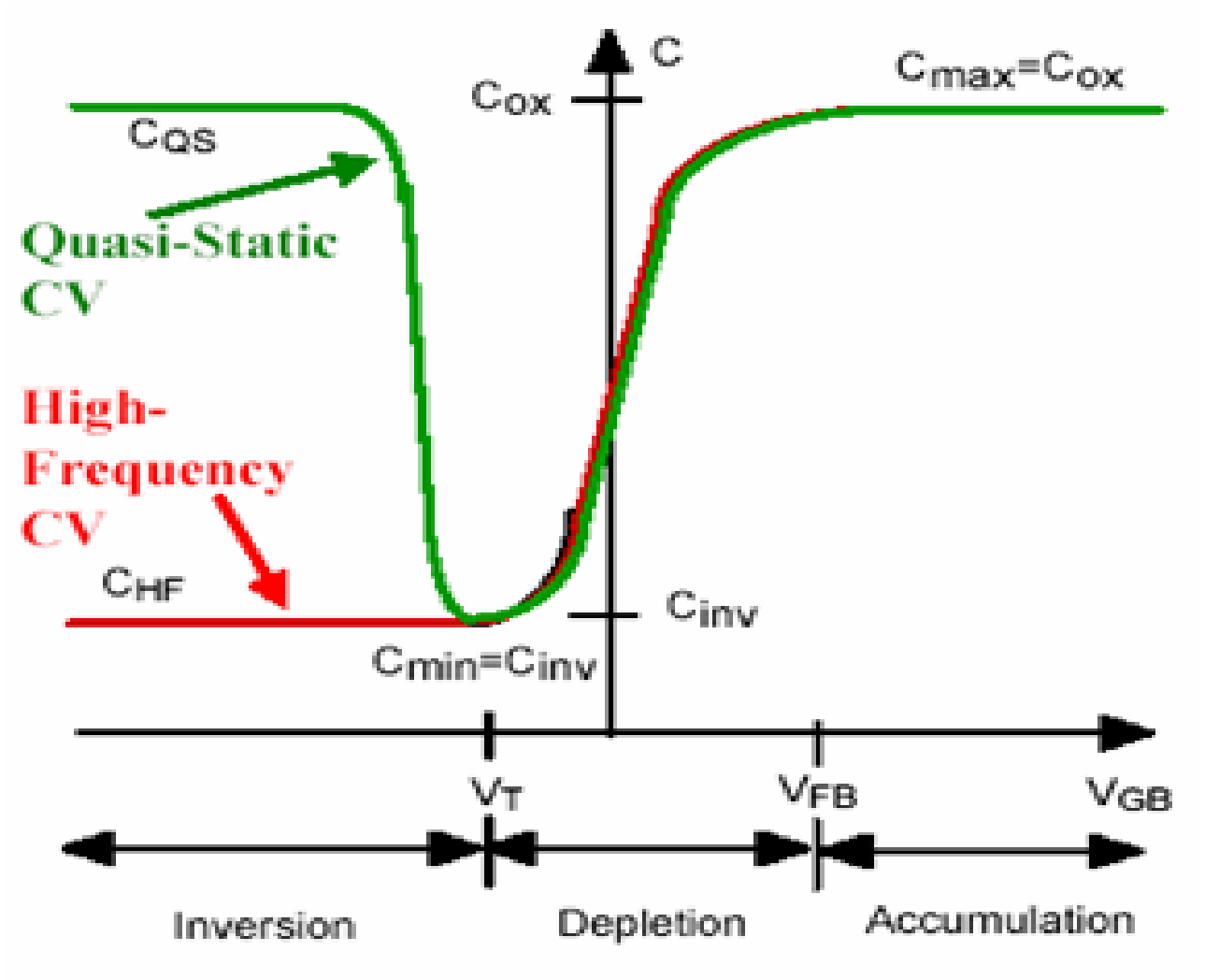
$$C_{s,max} = \varepsilon_{Si} / x_s$$

Depletion Layer Thickness

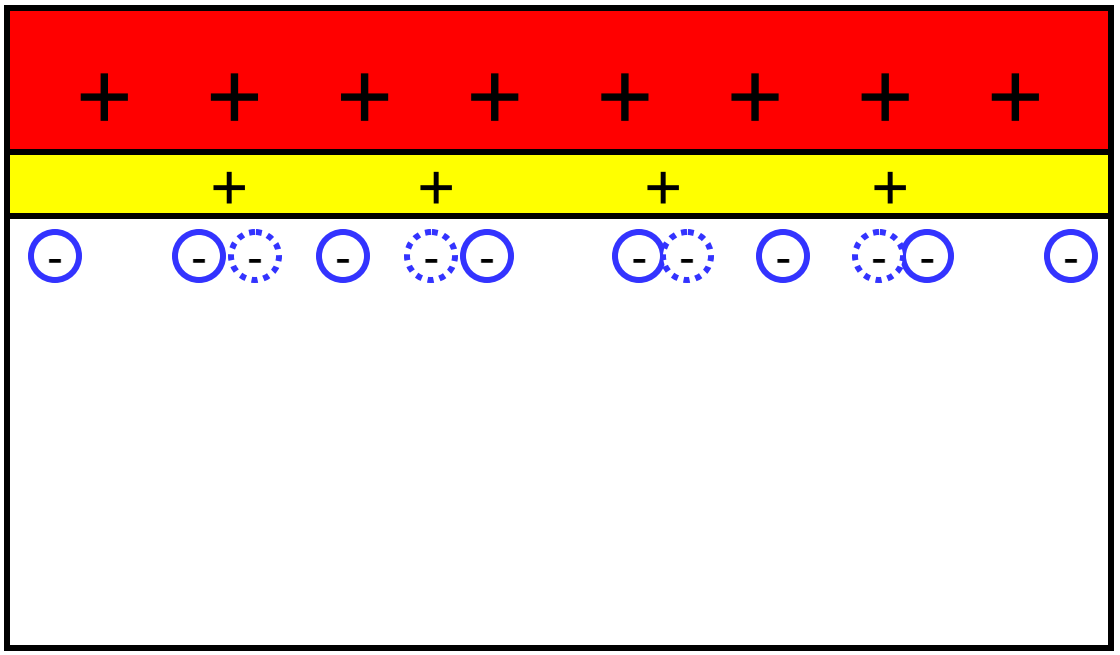


$$C_s = \varepsilon_{Si} / x_s$$

C-V


C
Cox
Cmax=Cox
CQS
Quasi-Static
CV
High-
Frequency
CV
CHF
Cinv
Cmin=Cinv
VT
VFB
VGB
Inversion
Depletion
Accumulation

Effect of Oxide Charge



A net shift in C-V curve:

Need to add more negative charge (voltage) to invert surface

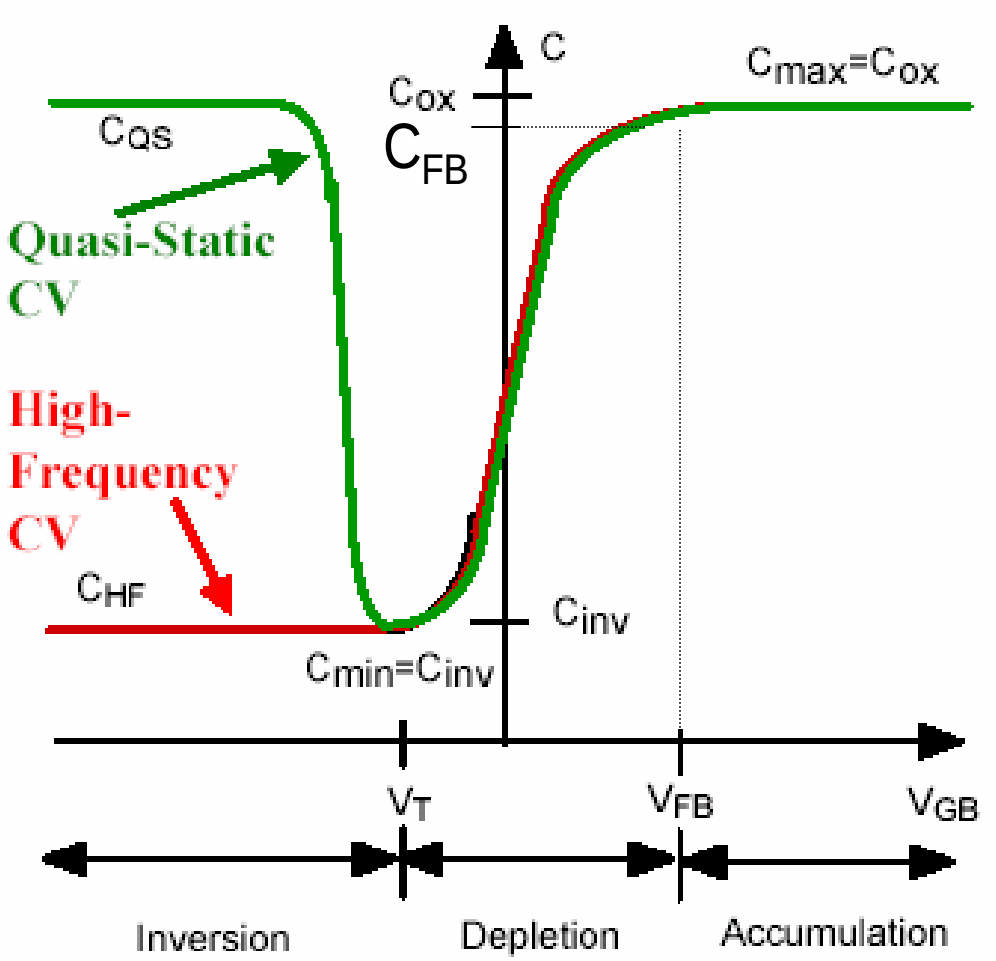
MOS Capacitance Measurement

Three measurements

- C_{ox}
- C_{min}
- V_{FB}

Produce

- t_{ox}
- N_D
- Q_f



Ref: A. Akinwande

C-V Analysis: Inversion

$$C^*_{\min} = \frac{\left(C^*_{ox} C^*_S\right)}{C^*_{ox} + C^*_S}$$

where C_s = semiconductor capacitance:

$$C^*_S = \sqrt{\frac{q\varepsilon_S N_D}{2\left(2\left|\Phi_F\right|\right)}}$$

and

$$\Phi_F = \left(\frac{kT}{q}\right)\ln\left(\frac{N_D}{n_i}\right)$$

Can extract N_D

C-V Analysis: Flatband

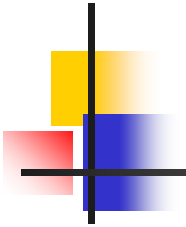
$$C_{FB}^{*} = \frac{1}{\frac{1}{C_{ox}^{*}} + \sqrt{\frac{kT}{q^2 \varepsilon_S N_D}}}$$

$$V_{FB} = \Phi_{MS} - \left(\frac{Q_F}{C_{ox}^{*}}\right)$$

$$\Phi_{MS} = \left(\frac{kT}{q}\right)\ln\left(\frac{N_D}{ni}\right) - \left(\frac{kT}{q}\right)\ln\left(\frac{N_C}{ni}\right)$$

$$= \left(\frac{kT}{q}\right)\ln\left(\frac{N_D}{N_C}\right)$$

Can extract Q_f



Summary

- Measurements - *Extraction*
  - Substrate Resistivity - *Substrate Doping*
  - Oxide Thickness
  - Poly Thickness
  - Poly Sheet Resistivity – *Poly Doping, Effective Mobility*
  - C-V (multiple areas) – *Oxide Thickness, Substrate Doping, Flatband Voltage (Fixed Charge)*
- Comparisons/Discussion
  - Oxide Thickness – Theory, C-V
  - Substrate Doping – Resistivity, C-V
  - Poly mobility – Expectations (relative to single crystal)
  - Flatband(Fixed Charge) – Expectations (sign and magnitude)