6.301 Solid State Circuits

Recitation 4: Fairchild μA733 Video Amplifier
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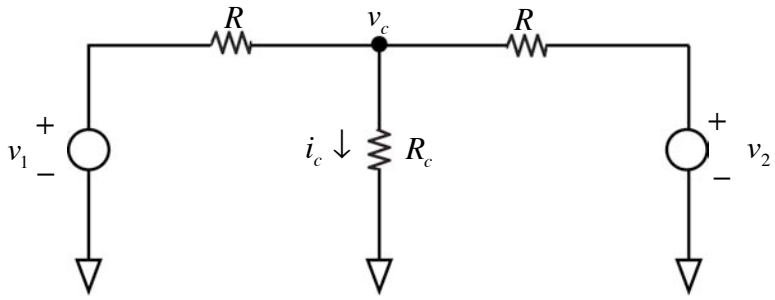
Today we're going to get some experience studying a relatively large analog system (large compared to 1- or 2- transistor stages): the μA733 of Fairchild Semiconductor. It is a fully differential video amplifier, by which we mean that it has differential inputs and outputs. Let's pause to remind ourselves of the whole differential vs. common-mode concept.

CLASS EXERCISE
Consider the following network:



1) Using superposition, write v_c and i_c in terms of v_1, v_2, R and R_c.
2) Simplify your expressions for the special case of $v_1 = -v_2$.

(Workspace)

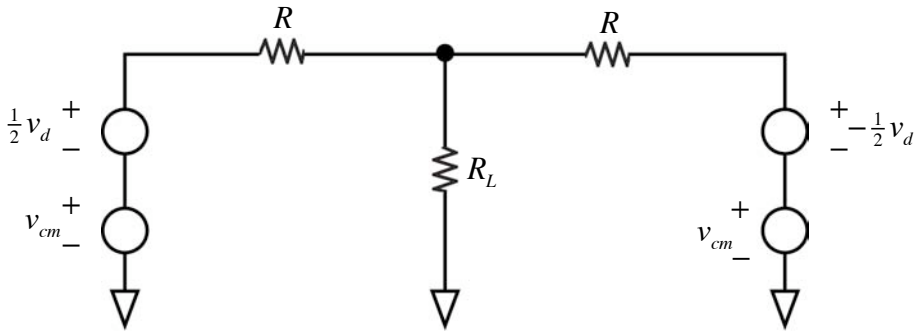
So for purely differential drive, we say that the node v_c is a "differential ground." Linearity allows us to write any v_1, v_2 as

$$v_1 = v_{cm} + \tfrac{1}{2} v_d$$
$$v_2 = v_{cm} - \tfrac{1}{2} v_d$$

where

$$v_{cm} = \tfrac{1}{2}(v_1 + v_2),\ v_d = v_1 - v_2$$

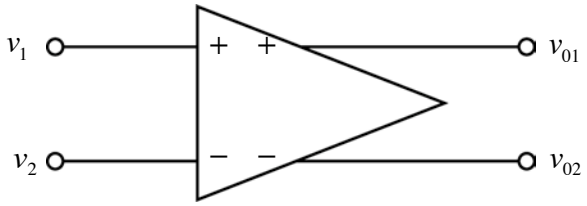
Our schematic becomes



And "half-circuit" analysis is nothing more than an expression of superposition. For the common-mode half-circuit, we set v_2 to zero and calculate responses. For the differential half-circuit, we set v_{cm} to zero.

Now let's look at the μA733 differential video amplifier.

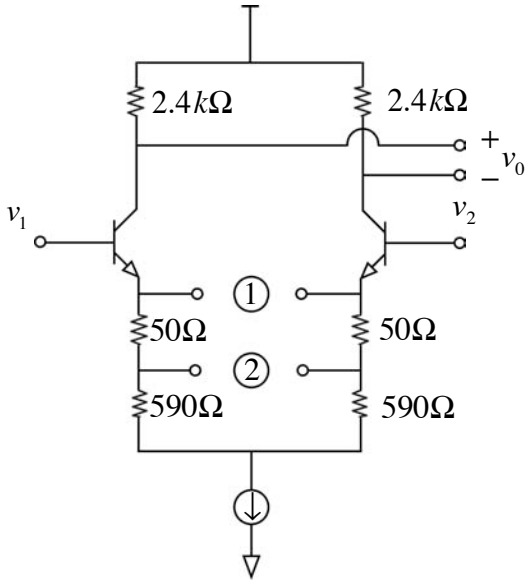
"Fully Differential"



Selectable Voltage Gain:	400	100	10
Corresponding Bandwidth:	40 MHz	90 MHz	120 MHz
Corresponding Input Resistance:	$4k\Omega$	$30k\Omega$	$250k\Omega$

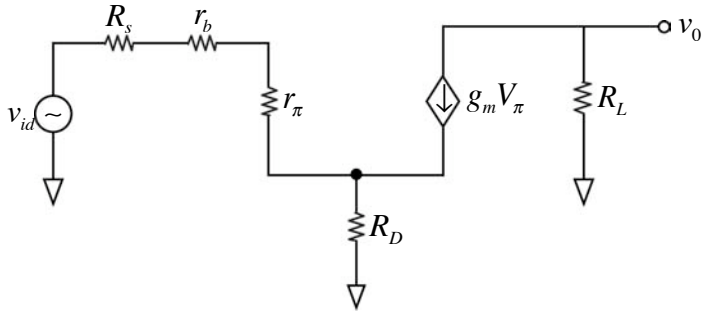
How do we do the selection? It's all done with the input stage…

Input stage:



- Shorting terminals (1) gives highest gain.
- Shorting terminals (2) gives medium gain.
- Leaving both open gives lowest gain.
- Single external resistor across terminals (1) allows continuous selection of gain by user.

Why does this work? The differential half-circuit of this input stage looks as follows:

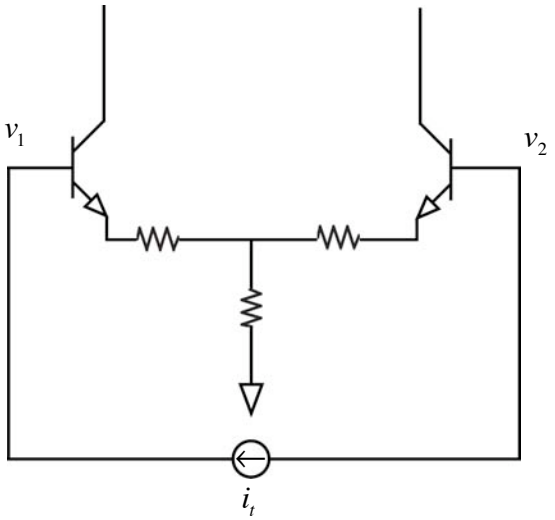


This is a familiar circuit:

$$a_{vd} \approx \frac{g_m R_L}{1 + g_m R_D} \approx \frac{R_L}{R_D}$$

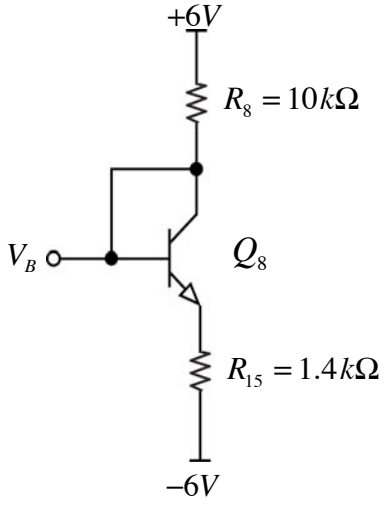
In the μA733, shorting out terminals (1) or (2), or connecting a resistor across (1), varies R_D. This is why the gain changes.

What about the input resistance? It's important to remember that the input resistance is twice the half-circuit input resistance. This is most easily seen by applying a differential test current source:



$$v_1 = i_t R_{HALF} \rightarrow v_t = v_1 - v_2 = 2i_t R_{HALF} \rightarrow R_{IN} = 2R_{HALF}$$
$$v_2 = -i_t R_{HALF}$$

Next, let's look at the bias point calculation. The right place to focus your attention to start this problem is on the "column" that contains Q_8:

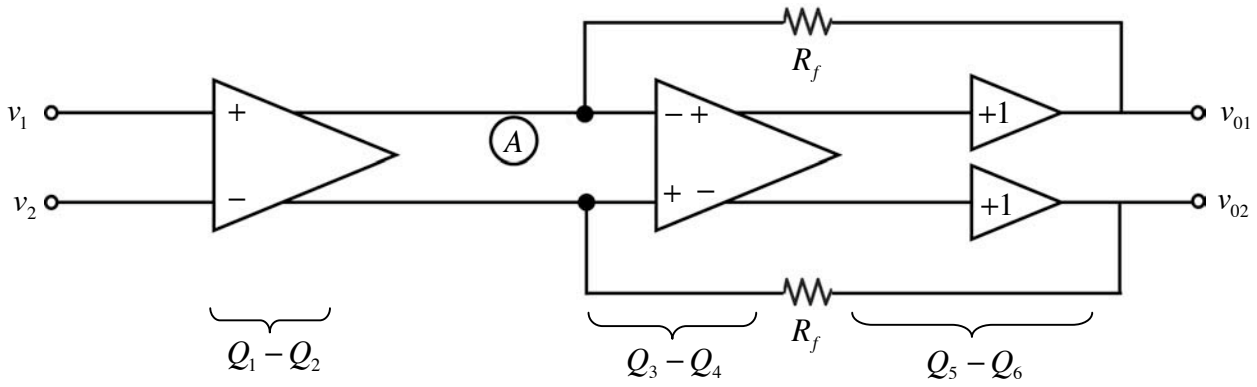


$$I_{C8} = \frac{12V - 0.6V}{10k\Omega + 1.4k\Omega} = 1mA$$

$$V_B = -6V + I_C R_{15} + V_{BE} = -4V$$

A very reasonable question to ask, when looking at a circuit with this many transistors is: How did I know to start there? The answer, of course, is experience. But one way to get that experience is to try starting a bias point calculation somewhere else in the circuit. See if you can make it work…

There is much more analysis to be done, and the course reader does an excellent job of getting through the details. Here, let's see if we can get some insight into why the original designers might have gone with this topology:



If we look in the course reader, we'll see that the gain of the amplifier formed by $Q_3 - Q_4$ is on the order of 100. The data sheet specs the output swing at V_{p-p}. What this means is that the differential voltage swing at point (A) is only $47mV_{p-p}$ …it is a low-swing node!

This helps two things:

(1) It allows for a larger common-mode input range.
(2) Since there is no gain from the bases of $Q_1 - Q_2$ to their collectors, the $C_\mu s$ of these devices do not get Miller multiplied. This helps to make it a high-bandwidth part.

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