MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.374: Analysis and Design of Digital Integrated Circuits
Problem Set # 3

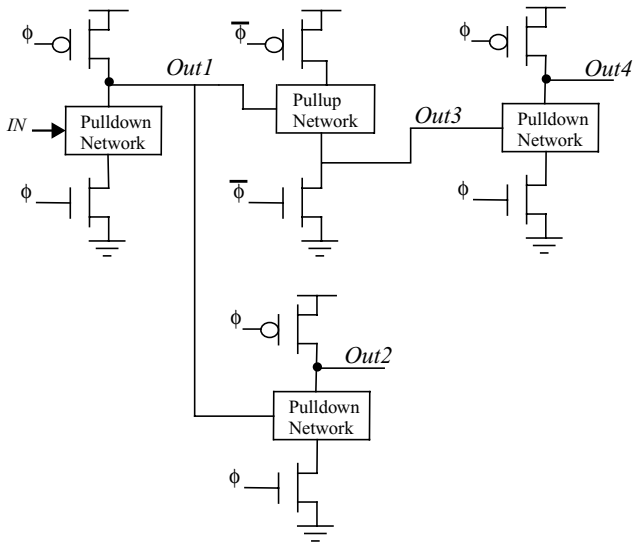
Fall 2003

Issued: 9/30/03
Due: 10/14/03

For these problems you can use the process parameters for the 0.25 technology- see the Process Parameters file in the assignments section.

Problem 1: Dynamic Logic I

Consider the conventional N-P CMOS circuit below in which all precharge and evaluate devices are clocked using a common clock ϕ and its complement. For this entire problem, assume that the pulldowown/pullup network is simply a single NMOS/PMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge time, evaluate time, and propagation delay of the static inverter are all $T/2$. Assume that the transitions are ideal (zero rise/fall times)



a) Do any problems occur when the input makes a 0->1 transition? What about a 1->0 transition? If so, describe what happens and insert one inverter somewhere in the circuit to fix the problem.

b) For your corrected circuit, complete the timing diagram for signals Out_1, Out_2, Out_3 and Out_4, when the *IN* signal goes high before the rising edge of the clock ϕ. Assume that the clock period is 10 T time units.

b) Suppose that there are no evaluate switches at the 3 latter stages. Assume that the clock ϕ is initially in the precharge state (ϕ=0 with all nodes settled to the correct precharge states), and the block enters the evaluate period (ϕ=1). Is there a problem during the evaluate period, or is there a benefit? Explain.

c) Assume that the clock ϕ is initially in the evaluate state (ϕ=1), and the block enters the precharge state (ϕ = 0). Is there a problem, or is there any benefit, if the last three evaluate switches are removed? Explain.

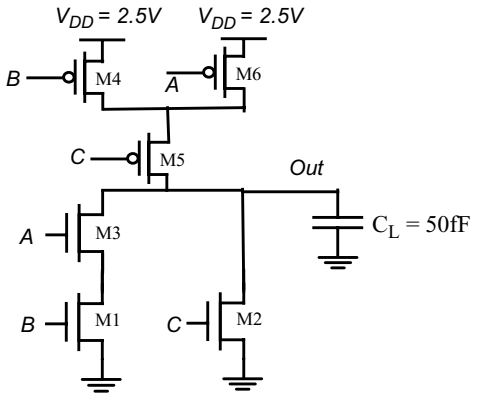
Problem 2: Leakage Power

Consider the circuit shown below:

a) What is the logic function implemented by this circuit? Assume that all devices (M1-M6) are 0.5µm/ 0.25µm.

b) Let the drain current for each device (NMOS and PMOS) be 1µA for NMOS at $V_{GS}= V_{Tn0}$ and PMOS at $V_{GS}= V_{Tp0}$. What input vectors cause the worst case leakage power for each output value? Explain (state all the vectors, but do not evaluate the leakage). Ignore DIBL**.**

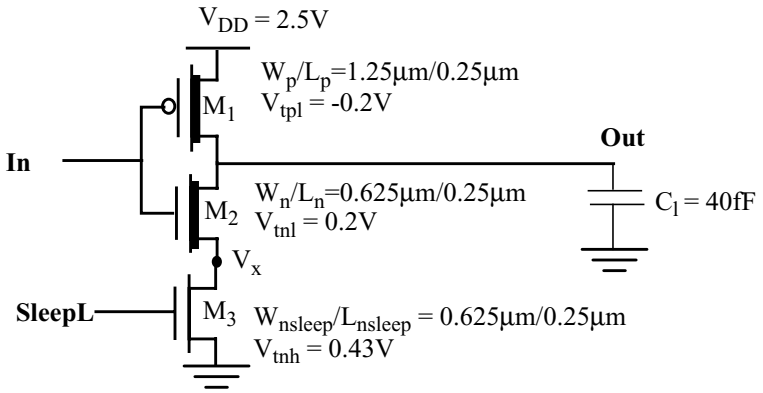
c) Suppose the circuit is active for a fraction of time *d* and idle for *(1-d)*. When the circuit is active, the inputs arrive at 100 MHz and are uniformly distributed ($Pr_{(A=1)} = 0.5$, $Pr_{(B=1)} = 0.5$, $Pr_{(C=1)} = 0.5$) and independent. When the circuit is in the idle mode, the inputs are fixed to one you chose in part (b). What is the duty cycle *d* for which the active power is equal to the leakage power?



Problem 3: Multi Threshold CMOS

Multi Threshold CMOS is a circuit technique that utilizes multiple threshold devices to provide both low leakage and high performance operation. The following problem explores some of the issues involved in MTCMOS circuits, although a more realistic circuit would be more complicated (like an adder or multiplier) instead of the single inverter shown below. For hand calculations, ignore body effect, lambda, and parasitic capacitances.

In the sleep mode, M3 is turned off, and this high Vt device limits the subthreshold leakage current. On the other hand, when the circuit is active, M3 is turned on hard for fast switching operation. For the rest of the problem, assume that M3 is turned on. (i.e. $V_{SleepL} = V_{DD}$)



Parts a) through f) do not require HSPICE.

a) What is the desired region of operation for M3 during the active mode?

b) Calculate the effective resistance looking into the drain of transistor M3.

c) Now assume the effective resistance of M3 is 0. What is the peak current (saturation current) that discharges C_l during an output high to low transistion?

d) What is the peak current taking into account the finite sleep resistance (computed in part b)

e) As W_{nsleep} increases, qualitatively how does t_{PHL} vary? How does t_{PLH} vary?

f) If there is a large parasitic capacitance at node Vx, what is the effect on switching performance?

For Hspice simulations use the models' file "logiclvt.l". Include two .lib statements, one with TT and one with TT_LVT and use nchlvt, pchlvt, and nch as the three device types in your netlist.

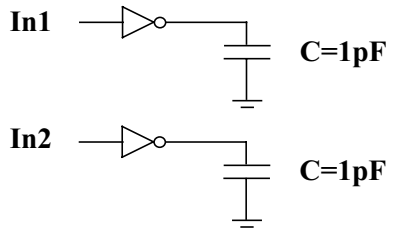
g) Using HSPICE, simulate the circuit for varying Wnsleep values of (0.625u, 1.5u, 3u, 5u, 7u, 9u, 11u). Turn in plots showing output voltage as a function of time and Vx as a function of time (with the varying Wnsleep curves superimposed on the same graph). Note if done correctly, HSPICE need only be run once. For the input specification, use the piecewise linear option: "Vin node1 node2 pl 0v 0n, 0v 2.5n, 2.5v 2.6n, 2.5v 7.5n, 0v 7.6n"

h) Plot t_{PHL} and t_{PLH} for each of these choices of Wnsleep

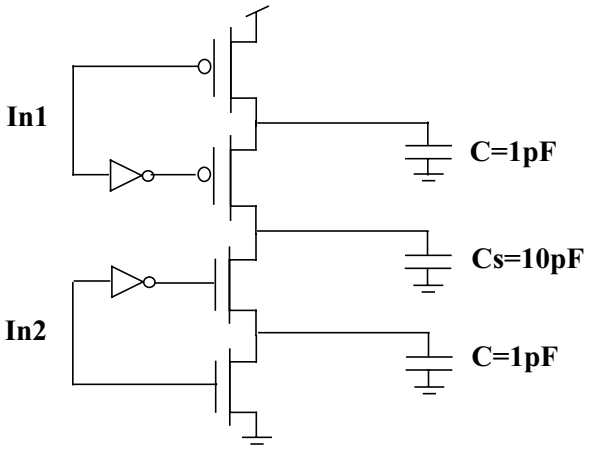
Problem 4: Low-Swing Bus Drivers

Consider the two possible bus driver circuits shown below:

Use 0.25 um technology: VDD=2.5 V



Circuit A



Circuit B

a) First consider circuit A. Assume an ideal inputs with zero rise time are available. Assuming Wp/Wn=3, find the minimum sized inverters such that tp will be less than 10% of the period for switching frequencies of 10 MHz, 100 MHz, and 1 GHz. (To make this easy, you can specify wn='0.375u*scale' and wp='1.125u*scale', specify the areas and perimeters similarly, and just vary the parameter 'scale'.) What is the leakage power consumed by inverters of each of these sizes when the input is low? What is the average total power consumed by the 2-bit bus if the inputs are tied together and switch at a frequency of 100 MHz? (For this very last question, just give a hand calculation based on switching power only and neglecting parasitics.)

b) Circuit B shows a simplified version of a purposed low-swing bus driver circuit. ["Low-swing charge recycle bus drivers" Karlsson, M.K.; Vesterbacka, M.; Wanhammar, L.; Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on , Volume: 2 , 31 May-3 June 1998; Page(s): 117 -120 vol.2] Explain how this circuit works. Theoretically, what should be the percentage power saved by using this circuit instead of Circuit A?

c) Now simulate Circuit B with the inputs tied together and switching at 100 MHz. Size the NMOS and PMOS as above and with scale=10. Be sure to initialize Cs to VDD/2 using a .ic statement. In a real circuit you would probably need to use progressively scaled buffers, but for this case you may assume that you have IN1, IN2 and their complements available at the gate inputs with zero rise/fall times. (This means you DO NOT need to implement the two inverters at the input.) How much power do we actually save by using this low-swing driver? Submit your output waveform.

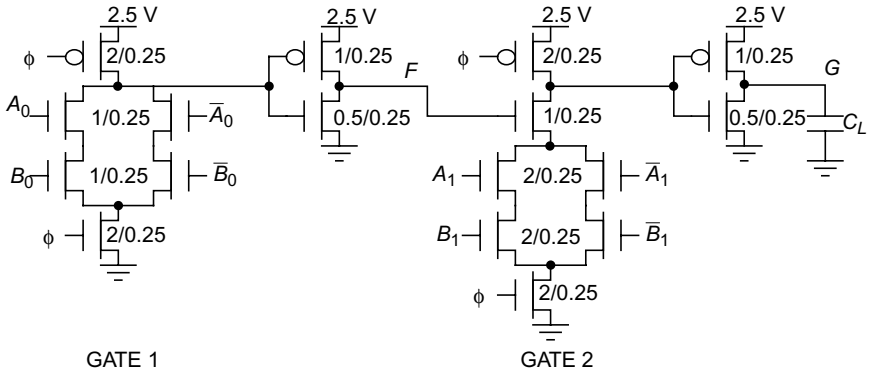
d) What problem might occur in Circuit B if the two inputs had different activity factors?

Problem 5: Dynamic Logic II

The figure below shows a dynamic CMOS circuit in Domino logic. In determining source and drain areas and perimeters, you may use the following approximations: $AD = AS = W \times 0.625\mu m$ and $PD = PS = W + 1.25\mu m$. Assume 0.1 ns rise/fall times for all inputs, including the clock. Furthermore, you may assume that all the inputs and their complements are available, and that all inputs change during the precharge phase of the clock cycle.

a) What Boolean functions are implemented at outputs F and G? If A and B are interpreted as two-bit binary words, $A = A_1A_0$ and $B = B_1B_0$, then what interpretation can be applied to output G?

b) Which gate (1 or 2) has the highest potential for harmful charge sharing and why? What sequence of inputs (spanning two clock cycles) results in the worst-case charge-sharing scenario? Using SPICE, determine the extent to which charge sharing affects the circuit for this worst case.



c) In part c you determined which gate (1 or 2) suffers the most from charge sharing. Add a single 2/0.25 PMOS precharge transistor (with its gate driven by the clock ϕ and its source connected to V_{DD}) to one of the nodes in that gate to maximally reduce the charge-sharing effect. What effect (if any) will this addition have on the gate delay? Use SPICE to demonstrate that the additional transistor has eliminated charge sharing for the previously determined worst-case sequence of inputs.

d) For the new circuit (including additional precharge transistor), find the sequence of inputs (spanning two clock cycles) that results in the worst-case delay through the circuit. Remember that precharging is another factor that limits the maximum clocking frequency of the circuit, so your input sequence should address the worst-case precharging delay.

e) Using SPICE on the new circuit and applying the sequence of inputs found in part (d), find the maximum clock frequency for correct operation of the circuit. Remember that the precharge cycle must be long enough to allow all precharged nodes to reach ~90% of their final values before evaluation begins. Also, recall that the inputs (A, B and their complements) should not begin changing until the clock signal has reached 0 V (precharge phase), and they should reach their final values before the circuit enters the evaluation phase.

Problem 6: Dynamic Power

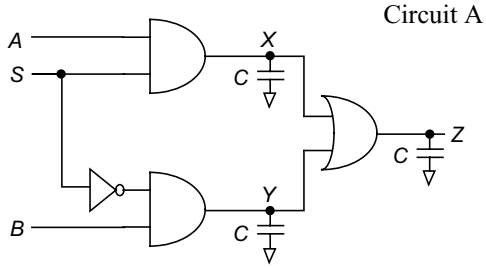
For parts a and b of this problem, assume independent, identically-distributed uniform white noise inputs.

a) What logical function is implemented by the Circuit A? Does this schematic contain reconvergent fan-out? Explain your answer. Find the exact signal (P_1) and transition ($P_{0 \rightarrow 1}$) formulas for nodes X, Y, and Z for: (1) a static, fully complementary CMOS implementation, and (2) a dynamic CMOS implementation. Assume an np-CMOS implementation with an n-tree first stage.

b) Compute the switching power consumed by Circuit A, assuming that all significant capacitances have been lumped into the three capacitors shown in the figure, where C = 0.3 pF. Also, assume that VDD = 2.5 V and that input events occur at a frequency of 100 MHz. Perform this calculation for a static, fully-

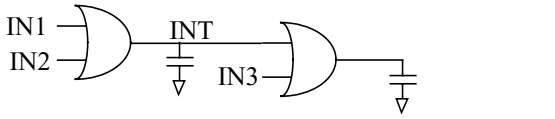
complementary CMOS implementation and a dynamic CMOS implementation. Assume np-CMOS again for the dynamic implementation, but find the power for both orders of trees.

Circuit A



c) Now consider the implementation of a 3-input OR gate shown in Circuit B. Assume that you have 3 inputs A, B, and C and where P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.1. For a static CMOS implementation of this circuit and neglecting any glitches that may occur, what is the best order to place these inputs in order to minimize power consumption? What is the activity factor at the internal node (INT) in this case? What is the worst order and the activity factor of the internal node in this case?

Circuit B



Problem 7: Dynamic Logic III

Consider the circuit shown below:

a) Give the logic function of *x* and *y* in terms of *A*, *B*, and *C*. Sketch the waveforms at *x* and *y* for the given inputs. Do *x* and *y* evaluate to the values you expected from their logic functions? Explain.

b) Redesign the gates using *np*-CMOS to eliminate any race conditions. Sketch the waveforms at *x* and *y* for your new circuit.