Superconducting Digital Circuits (overview)

Outline

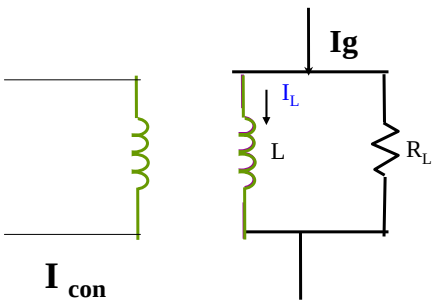
1. Josephson Switches, Memories and Characteristic Times

2. Voltage State Logic

3. Single Flux Quantum (SFQ) Logic

November 1, 2005

Cryotron Switch



Current goes through the SC as I_L
until I_{con} causes the SC to become normal,
sending the current through R_L

Characteristic time is L/R = 20 nH/1 ohm = 20 nsec

Cryotron Memory

Cryotron: Dudley Buck in 1956 at MIT
Used materials which had an Hc = 100 g such has Nb-Ta and Pb-Sn alloys

Image removed for copyright reasons.

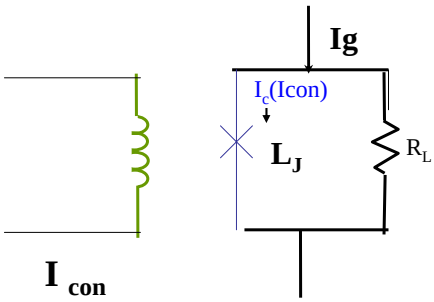
Please see: Figure 3.12, page 90, from Orlando, T., and K. Delin. *Foundations of Applied Superconductivity*. Reading, MA: Addison-Wesley, 1991. ISBN: 0201183234.

0 to 1 Storage

Image removed for copyright reasons.

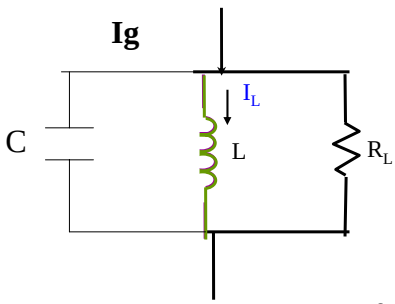
Please see: Figure 3.13, page 91, from Orlando, T., and K. Delin. *Foundations of Applied Superconductivity*. Reading, MA: Addison-Wesley, 1991. ISBN: 0201183234.

Josephson Switches



Current goes through the SC as I_c(Icon)
until I_{con} causes the SC to become normal, sending the current through R_L

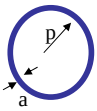
Josephson Switching Times



The switching times is the slower of $\mathbf{t_J}$ and $\mathbf{t_{RC}}$
Depending on whether $\beta c < 1$ **or** $\beta c > 1$

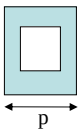
Note that the shortest switching time is when $\beta c > 1$
Where t_J is about $h/\pi\Delta = 0.2$ ps

Superconducting Parameters



$$L[\mathrm{nH}] = p[\mu\mathrm{m}] \ln\frac{p}{a}$$

$$C_0 = 50\,\mathrm{fF}/\mu\mathrm{m}^2$$



$$L[\mathrm{nH}] = 1.2\,p[\mu\mathrm{m}]$$

$$R_n[\Omega] = \frac{190}{A[\mu\mathrm{m}^2]\,J_c[kA\mathrm{cm}^2]}$$

$$L[\mathrm{nH}] = 1.2\,(2\lambda + d)[\mu\mathrm{m}]$$

$$\tau_J[\mathrm{ps}] = 0.15\left(\frac{R_n}{R_{sh}}\right)$$

$$\tau_{RC}[\mathrm{ps}] = \frac{7.5}{J_c[kA/cm^2]}\left(\frac{R_{sh}}{R_n}\right)$$

$$L_J[\mathrm{nH}] = \frac{300\mathrm{pH}}{I_c[\mu\mathrm{A}]}$$

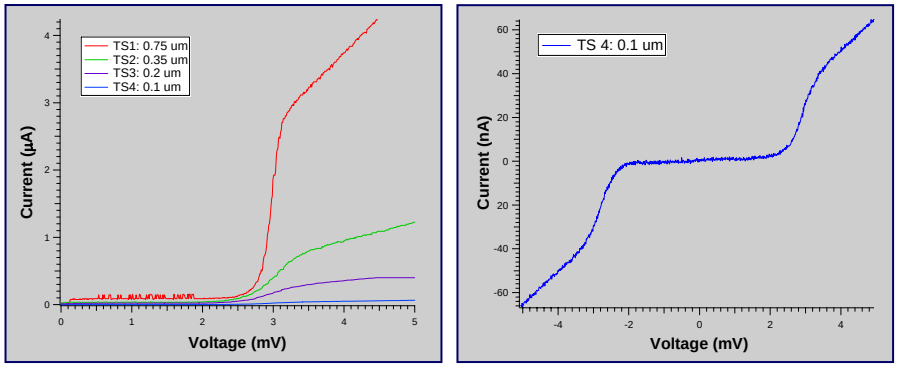
$$\beta_c = \frac{50}{J_c[kA/cm^2]}\left(\frac{R_{sh}}{R_n}\right)^2$$

Optimal Junction Size and Shunt Resistors

Image removed for copyright reasons.

Please see: Figure 6.3, page 254, from Kardin, A. *Introduction to Supercomputing Circuits*. 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

DSM Process Testing at 4K:
JJ I-V Traces



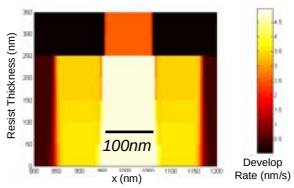
- **DSM JJs @ T=4K**
  - **Junction sizes down to 0.07 μm**
    Qubits and RSFQ applications
  - **High subgap resistance**

Robust Shadow-Mask Evaporation via Lithographically Controlled Undercut**

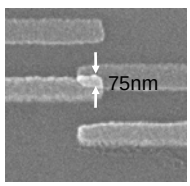
Bryan M. Cord, José Aumentado*, Terry P. Orlando, **Karl K. Berggren**
Massachusetts Institute of Technology, Cambridge, MA
* National Institute of Standards and Technology, Boulder, CO

See poster**

- Suspended shadow-mask evaporation relies on the ability to fabricate large undercut regions in photoresist
- Undercut in a PMMA/PMGI bilayer can be accurately defined using electron-beam lithography, rather than development time
- The properties of PMGI have been extensively characterized in order to model the undercut process
- Improved control of undercuts has increased the robustness and resolution of the suspended shadow-mask evaporation process



Simulation of the development rate profile for a 100nm line with 100nm defined undercut in PMMA/PMGI



SEM image of a Josephson junction with an area of ~0.007 μm²

Transient Response for $\beta_c >> 1$

Image removed for copyright reasons.

Please see: Figure 6.4, page 256, from Kardin, A. *Introduction to Supercomputing Circuits*. 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

Transient Response for $\beta_c << 1$

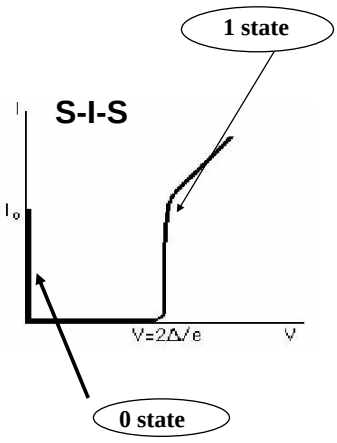
Image removed for copyright reasons.

Please see: Figure 6.5, page 257, from Kardin, A. *Introduction to Supercomputing Circuits*. 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

Delay-Power Graph

Image removed for copyright reasons.

Please see: Figure 9.19, page 480, from Orlando, T., and K. Delin. *Foundations of Applied Superconductivity.* Reading, MA: Addison-Wesley, 1991. ISBN: 0201183234.



2. Voltage State Logic

1. Underdamped Junctions $\beta_c >> 1$
2. Can use unshunted junctions
3. Must induce a "switch" from 0 state to 1 state by changing the critical current
4. Once in the 1 state, must drive critical current to zero to reset

Transient Response for $\beta_c >> 1$

Image removed for copyright reasons.

Please see: Figure 6.4, page 256, from Kardin, A. *Introduction to Supercomputing Circuits*. 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

Voltage-State Switching

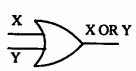
Image removed for copyright reasons.

Please see: Figure 6.7, page 261, from Kardin, A. *Introduction to Supercomputing Circuits*. 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

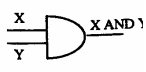
Voltage-State Logic Gates

Image removed for copyright reasons.

Please see: Figure 6.8, page 262, from Kardin, A. *Introduction to Supercomputing Circuits*. 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.



$$I_X + I_b > 2I_c \quad \text{or} \quad I_Y + I_b > 2I_c$$



$$I_X + I_Y + I_b > 2I_c$$

Voltage-State Memory

Image removed for copyright reasons.

Please see: Figure 6.9, page 263, from Kardin, A. *Introduction to Supercomputing Circuits*. 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

3. Single Flux Quantum (SFQ) Logic

Image removed for copyright reasons.

Please see: Figure 5.45a, page 243, from Kardin, *A. Introduction to Supercomputing Circuits.* 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

Image removed for copyright reasons.

Please see: Figure 5.42, page 237, from Kardin, *A. Introduction to Supercomputing Circuits.* 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

SFQ Pulse (a vortex)

$$\Lambda = \sqrt{\frac{L_J}{L}}$$

Size of a vortex in a paralle array,

SFQ pulse confined to one cell Λ = 1

Transient Response for $\beta_c << 1$

Image removed for copyright reasons.

Please see: Figure 6.5, page 257, from Kardin, *A. Introduction to Supercomputing Circuits.* 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

SFQ: The Josephson Transmission Line

Image removed for copyright reasons.

Please see: Figure 6.15a, page 271, from Kardin, *A. Introduction to Supercomputing Circuits.* 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

Vortex (fluxon) moving to the right

Anit-Vortex (anti-fluxon) moving to the left

SFQ Splitter

Image removed for copyright reasons.

Please see: Figure 6.15b, page 271, from Kardin, *A. Introduction to Supercomputing Circuits.* 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

SFQ Memory Cell

Image removed for copyright reasons.

Please see: Figure 6.18a, page 275, from Kardin, *A. Introduction to Supercomputing Circuits.* 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.

SFQ Logic Gates

Images removed for copyright reasons.

Please see: Figure 6.19, page 277, from Kardin, *A. Introduction to Supercomputing Circuits.* 1st ed. New York, NY: Wiley-Interscience, March 11, 1999. ISBN: 0471314323.